Contents

1
Atom chip fabrication

Ron Folman, Philipp Treutlein, and Jörg Schmiedmayer

1.1
Introduction

One of the key promises of atom chips is the building of a robust quantum laboratory by miniaturizing and integrating quantum optics and atomic physics tools on a single device, on a chip [1–3]. This vision follows the path taken previously by the micro electronics and micro optics fields. The advantages and strengths of the specific field, in our case quantum optics in atomic systems, are combined with the technological potential of microfabrication and (large scale) integration to build a robust platform for implementation of quantum operations. An important ingredient in developing such an integrated, microfabricated approach to manipulating atoms, molecules or ions is the fabrication of the devices. The possibilities to combine vastly different technologies is thereby a key factor. This creates the technological basis for combining the best of the different quantum worlds of photons, atoms and solid-state in a single integrated quantum device.

This overview of atom chip fabrication is organized as follows: We first discuss the challenges to be faced when starting to conceive and fabricate chips for the (quantum) manipulation of atoms. We then describe the various ingredients and the corresponding fabrication methods. We focus not only on the currently most active and successful areas - current carrying wires and integrated photonics, but also look at more visionary approaches, examples being superconducting chips or the manipulation of atoms with real nano structures such as carbon nano tubes.

Here we explicitly discuss the material engineering and fabrication of atom chips for the manipulation of neutral atoms, but the same concept of robustness and versatility through miniaturization and integration can also be applied to manipulate (polar) molecules, ions, or trapped electrons.

1.2 Fabrication challenges

In building atom physics based quantum devices on a chip, the challenge is not so much in micro and nano scale miniaturization, but rather in the integration of numerous technologies on the same device, and in the exceptional quality required from both the materials and the fabrication. Besides being UHV compatible, different requirements need to be addressed, depending on the specific application we have in mind.

- Current carrying wires are the workhorse of atom chips. Their key role is to provide magnetic fields for trapping and manipulation. These wires have to support high current densities, in some cases $> 10^7$ A/cm^2 [4,5], many orders of magnitude larger than in a light bulb. Ultra cold atoms are extremely sensitive to variations in the magnetic potential. These can be caused by non uniform current flow in the wires. Current flow deviations of $\sim 10^{-6}$ rad can be seen in 1d BEC experiments [6, 7]. A deviation of $> 10^{-4}$ rad makes a trap unusable for many experiments.

- Micro structured magnetic films and permanent magnets provide a very attractive way to create strongly confining micro traps at very high integration density [8–12]. One of the key issues in fabrication thereby is again the homogeneity of the magnetic materials [13].

- Radio-frequency (RF) and microwave (MW) fields complement the static magnetic trapping potentials [14–20]. Coupling two different ground states creates dressed state potentials similar to optical dipole potentials. The wire structures and the substrates need to be chosen well to support precise microwaves.

- Electric fields offer a route to detailed structuring and manipulation [21]. At the micron scale the substrates and the fabricated structures have to withstand the large electric fields created at even moderate voltages.

- Multi layer chips [20,22,23] are very instrumental. In an integrated atom chip, large structures (10 to 500 μm) for the initial trapping and cooling of atoms have to be combined with functional structures on the (sub) micrometer scale to achieve controlled manipulation at a length scale where tunnel coupling between sites becomes important. Furthermore, the versatile application of electric and magnetic potentials requires the crossing of wires on the chip without contact.

- In many applications the chip surface needs to be a high quality mirror, be it for cooling and accumulating the atoms in a mirror MOT or for imaging atoms close to the surface. Furthermore, reflection of light

from the chip surface allows to integrate optical dipole traps and optical lattices on the atom chip [24]. This puts very stringent requirements on the quality of the mirror surface.

- By integrating micro optics and fiber optics on the atom chip [25, 26] one can incorporate optical micro manipulation and efficient detection of atoms. The fabrication methods for the optics have to be compatible with the other processes. Integrating fully tunable optical micro cavities pose an even larger challenge [27].

- Integration of superconducting elements on the chip will require compatibility with cryogenics.

- The atom chip is an ideal platform to integrate other solid state quantum devices like Micro-Electro-Mechanical systems (MEMs) [28,29], micro lenses and holes, miniature high finesse cavities, current carrying molecules or nano magnets, crystalline materials, etc. with the atomic physics on the chip. Connecting atoms to superconducting qubits [30,31] through circuit CQED [32, 33] will even require to go to mK temperatures.

- Looking further into the future one can think of integrating more complex devices onto the chips like on board light and particle sources, miniature vacuum volumes and pumps, etc. (see last figure of this chapter) to build an independent stand alone device.

With all these diverse science possibilities each chip has an individual design, tailored to the physics and functions it is required to perform. What is needed is an interplay between physics, material engineering and fabrication, and compatibility of the methods.

1.3 The substrate

The substrate onto which the atom chip is fabricated has to be compatible with the different fabrication techniques needed to implement the chip design and has to guarantee the robust operation of the device. For a comparison of different substrate materials see Table 1.1.

In general the most important physical properties for present day atom chips stem from the fact that one of the key functions is to accumulate, cool and manipulate ultra cold atoms using static or oscillating fields. The substrate of the atom chip has to support the wires, provide electrical insulation between them, and dissipate the heat generated in the wires. Therefore, a

substrate with high thermal conductivity, a high heat capacity, and an insulating surface is needed. A second important requirement, needed for smooth magnetic potentials, is the ease of high quality fabrication (few geometrical defects) and low wire surface roughness. This translates, for example, to very low surface roughness of the substrate.

A common substrate is a single crystal Si wafer in a (100) orientation with a thermal conductivity of $\sim$ 150 W/(mK) at room temperature. Wafers are typically $\sim$ 500 μm thick and polished with very small surface roughness, sufficient even for the smallest wires. They can be cleaved with a diamond scorer. Neither the resistivity of Si nor the 2 nm native oxide layer on the substrate are sufficiently insulating for controlling DC currents at the 10^{-5} level. Therefore the wafer is covered by a SiO_2 insulation layer which provides a DC resistance of > 40 MΩ between the wires. Since SiO_2 has a thermal conductivity of only 1.5 W/(mK), the insulating layer should be as thin as possible [5,34].

AlN is a non-toxic polycrystalline ceramic with an excellent heat conductivity of typically 180 W/(mK) at room temperature. Compared with Si, AlN is less brittle. It can be laser machined and easily cleaved with a diamond scorer. A polished AlN surface (specified surface roughness < 40 nm) has a significant residual roughness, with isolated defects of micrometer size. This is a problem if structures < 10 μm are desired.

Both AlN and Si are common substrate materials for microwave circuits. AlN has a dielectric constant of ε_r = 8.7 and a loss tangent of $\tan\delta < 1 \times 10^{-3}$

Material	Therm. cond. $Wm^{-1}K^{-1}$	Specific Heat J/KgK	ε_r	loss tang. 10 GHz 10^{-4}	Linear expans. $10^{-6}K^{-1}$	Density g cm^{-3}	Optical transm. nm
BeO	260-300	1000	6.7	30	8.4-9.0	2.86	
AlN	170-280	800	8.9	5	4.4-5.7	3.25	500-3000
Al_2O_3							
Macor	1.5	790	5.9		13	2.52	
Sapphire	35-40	700	9-11	0.2-0.8	5.8	3.99	200-5500
Alumina	26-35	900	9.6	1	8.0	3.9	
SiN	10 - 16	690	10		3.3	2.4	
SiO_2	1.46	700	3.9	1-10	0.54	2.2	180-2500
BK7	1.11				8	2.51	400-1400
Pyrex	1.13				3.25	2.23	300-2500
Polyimide	0.1-0.35	1090	3.4		30-60	1.42	
Diamond	900-2000	470	5.7	2	0.8	3.52	400-300000
GaAs	$\sim$ 55	330	10.9-12.9	<6	5.8	5.3	1500-14000
Si	80-150	700	11.7	<10	4.7-7.6	2.34	1200-15000
SiC	350	690	10.8	30	4.8	3.2	

Tab. 1.1 Room temperature properties of commonly used substrates for micro fabrication (data collected form a number of internet resources)

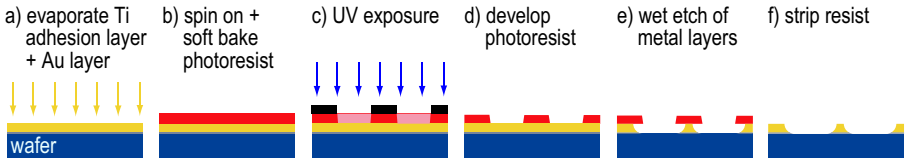

Fig. 1.1 Process steps of optical lithography (see text). The example uses a contact mask, a positive resist system, and pattern transfer to the metal layer by wet etching.

at 10 GHz. If only DC currents are used in the experiment, Si of any doping level can be employed as the substrate material. For microwave applications, however, it is very important to choose high-resistivity Si to avoid strong dielectric losses. A typical wafer has a resistivity of $\rho > 10^4 \Omega$cm, $\varepsilon_r = 11.9$, and $\tan\delta = 1 \times 10^{-3}$ at 10 GHz.

Other substrates commonly used in atom chip fabrication are GaAs, sapphire, alumina or SiO_2. Especially sapphire is interesting as a substrate for low temperature micro wave applications, where a loss tangent close to 10^{-6} has been observed. Sapphire is also interesting when using light, as it is transparent in the visible light range.

1.4 Lithography

In lithography, a pattern is transferred into a layer of resist on the chip surface. The patterned resist is subsequently used as a stencil for etching or depositing material. An extensive discussion of lithographic techniques can be found in [35]. In the following, we give a brief introduction to optical and electron beam lithography, which are most commonly used for atom chip fabrication.

1.4.1 Optical lithography

In optical- or photolithography, light is used for pattern transfer from a mask to a light-sensitive resist. The spatial resolution is therefore set by diffraction of light. Optical lithography is a parallel process which allows large chips to be structured in short time, making it the dominant technique in the semiconductor industry. A typical photolithographic process involves several process steps as illustrated in Fig. 1.1: *(a) substrate preparation – (b) spinning resist and soft baking – (c) exposure and postexposure treatment – (d) resist development – (e) transfer of the resist structure to the substrate – (f) resist stripping*. In the following, we discuss this process in more detail.

Masks for photolithography — The photomask is a flat piece of glass (transparent to UV light) carrying a thin absorbing metal pattern (e.g. a 100 nm thick Cr layer) on one side. Depending on the resist system, the pattern on the mask is either a light field or dark field image of the structure to be fabricated. In research laboratories, the most common technique is contact lithography, where the metal pattern on the mask is in direct contact with the photoresist layer during exposure. A *mask aligner* is used to align mask and substrate with respect to each other and expose them to UV light (often, mercury lamps with spectral lines near 400 nm are used). The direct contact of mask and resist can result in defects. An alternative are projection masks, which are imaged by a high-resolution lens system onto the resist. Many commercially available masks are fabricated by laser lithography, i.e. by writing the pattern with a laser beam of $\simeq 0.7$ μm spot size into a thin resist layer on the mask. Masks with smaller structures can be written by electron beam lithography (see below). For coarse structures (> 50 μm), the mask can be simply printed on a transparency. Laser lithography can also be used to avoid photomasks completely, by directly exposing the resist on each chip with the laser beam.

Substrate preparation — Lithography starts with a thorough cleaning of the substrate. Different (combinations of) wet or dry cleaning procedures are used, involving e.g. organic solvents in an ultrasonic bath, or a strong acid such as H_2SO_4, or an acid-oxidant combination (e.g. 'piranha etch'), or oxygen plasma cleaning. Subsequent to cleaning, some processes require deposition of homogeneous insulating and/or metal layers on the substrate. In the example of Fig. 1.1, the substrate is covered with a thin Ti adhesion layer and a gold layer, which will later be patterned by wet etching.

Spinning resist and soft baking — A spin coater is used to apply a photoresist layer of a desired thickness (ranging from a few 100 nm to a few 100 μm, depending on the resist system and application). The photoresist is an organic polymer sensitive to UV radiation. After spin coating, the resist layer is soft baked (prebaked) to remove solvents and promote adhesion to the substrate.

Exposure and postexposure treatment — The resist-coated substrate is aligned with respect to the photomask and subsequently illuminated with a well defined intensity of UV light for a controlled duration (typically a few seconds). Finding the proper exposure dose is an important task during optimization of the process. The UV light induces a chemical reaction in the exposed areas of the photoresist, altering the solubility of the resist in a solvent. If a *positive resist* is used, the exposed areas are rendered soluble. In a *negative resist*, the exposed areas are rendered insoluble. After exposure, certain resists require further treatments. For example, an *image reversal resist* requires a post-exposure bake and subsequent flood exposure with UV light, thereby turning the originally positive resist into a negative one. The choice of the resist system for a given application depends on many parameters, such as the

desired spatial resolution and resist thickness, the desired shape of the resist profile (positive vs. negative slope of the resist sidewalls, see section 1.5), and the chemical stability in subsequent processing steps.

Resist development — During development, the resist is selectively dissolved, usually by submerging and agitating the substrate in a liquid developer solution. This transforms the latent image formed during exposure into a resist pattern that will serve as a mask in further deposition or etching steps. Careful control of the development time and developer temperature is required to reproducibly obtain the desired resist profile. A mild oxygen plasma treatment can be useful to remove unwanted resist left behind after development. Furthermore, some applications require postbaking of the developed resist to improve stability.

Transfer of the resist structure to the substrate — Various methods exist to transfer the resist structure to the substrate, and the most common ones for atom chip fabrication are discussed in section 1.5 below. In the example of Fig. 1.1, wires are defined by a wet etch of the metal layers with aqua regia.

Resist stripping — In the last step of the photolithographic process, the resist is removed (stripped). Similar to the procedures for substrate cleaning, a sequence of steps involving organic solvents, acids, acids+oxidants, or plasma cleaning is used. The additional requirement is that the chemicals and procedures employed should not attack the desired structures.

Spatial resolution — The spatial resolution of contact lithography is limited by the near-field diffraction of light at the structures in the mask and thus decreases if there is a gap between the mask and the substrate. Consider photoresist of thickness t exposed with light of wavelength λ through a mask with a pattern of equal lines and spaces of periodicity $2w$. The theoretical resolution, i.e. the minimum linewidth resolved, is given by $w_{\mathrm{min}} = (3/2)\sqrt{\lambda(g + t/2)}$, where g is the gap between resist and mask [35]. To obtain high resolution, g has to be as small as possible. This means that edge beads and defects of the photoresist have to be avoided. The substrate has to be pressed against the mask. In a multi-layer process, the topology of the lower layers (if not planarized perfectly) will introduce gaps and thus decrease resolution. As an example, consider $\lambda = 400$ nm, $t = 1.5$ μm, and $g = 0$, which yields $w_{\mathrm{min}} = 0.8$ μm. In practice, achieving such high resolution is possible, but challenging. Routinely, $w > 2 - 3$ μm is achieved.

Resist bleaching is a phenomenon that allows one, to some extent, to enhance resolution beyond w_{min}. During exposure, the resist becomes more transparent to the illuminating light. This allows one to define narrow features in thick resist, i.e. the fabrication of structures with high aspect ratio.

1.4.2 Electron beam lithography

Electron beam lithography allows one to fabricate significantly smaller structures than optical lithography. Moreover, the electron beam has a large depth of focus, facilitating patterning of substrates with uneven topography. E-beam lithography is a serial technique in which a narrow electron beam is scanned across a resist layer pixel-by-pixel. The resolution is limited by electron scattering in the resist and substrate to typically $10 - 100$ nm, depending on resist thickness. The standard positive resist is polymethylmethacrylate (PMMA). Electron bombardment breaks the PMMA into fragments, the resulting shorter polymer chains are dissolved faster during development. Negative resists and multi-layer resist systems are available as well.

E-beam lithography is slow, and writing a complex pattern can easily take several hours, making the system prone to drifts and vibrations. Moreover, the size of the field that can be written without moving the substrate is typically only a few hundred μm, for larger areas stitching is necessary. Nevertheless, the superior resolution make e-beam lithography the method of choice in many applications. The basic steps involved in an electron beam lithography process are similar to those discussed in the previous section. During exposure with the e-beam, the substrate is mounted in a vacuum chamber. No physical mask is needed, the pattern is defined in computer software.

Optical and electron beam lithography are often combined. The smallest and most critical structures in the chip center are defined by electron beam lithography, while optical lithography is used in a separate process step for uncritical 'large-scale' structures such as lead wires and contact pads at the edge of the chip.

1.5 Metallic layers

Metallic wires, electrodes, or permanent magnets are the most commonly used structures on an atom chip. In the following we introduce the most important deposition and etching techniques used for the patterning of normal metals, discuss issues of roughness and homogeneity of the structures, and review the fabrication of structures out of special metals such as alloys, superconductors, semiconductors, and permanent magnets.

1.5.1 Deposition and etching

Resist patterns created by lithography can be transferred to the substrate by *additive* (deposition) or *subtractive* (etching) techniques. The two most com-

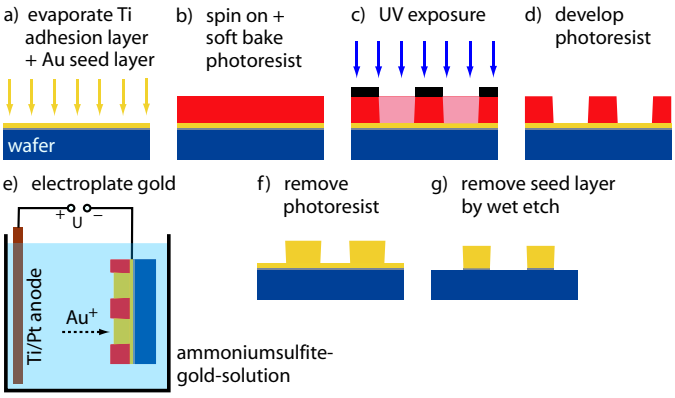

Fig. 1.2 Electroplating. The process steps are explained in the text.

monly used techniques for the fabrication of atom chip wires are additive techniques: electroplating and lift-off metallization.

1.5.1.1 Electroplating

Electroplating was among the first techniques used for atom chip fabrication [4, 36]. In this technique, the chip serves as the cathode of an electrolytic cell. Resist structures on the chip form a mold for the electroplated metal. Under an applied voltage, metal ions from the plating solution deposit on the areas not covered by resist. The amount of deposited material per unit time is controlled by the current flow. Electroplating is more time and material efficient than metal deposition through thermal evaporation or sputtering. It is therefore well suited also for structures with a thickness $\gg 1\mu$m. Furthermore, structures with high aspect ratio (wire height comparable to or higher than width) are easier to fabricate than with lift-off or etching techniques (see below). Electroplating is very versatile, it can also be used to fabricate vias and other non-planar structures [35]. A review of electroplating can be found in [37, 38], and its application to atom chips is discussed e.g. in [39–41].

Fig. 1.2 illustrates a basic gold electroplating process (a detailed recipe can be found in [41]). (a) After substrate cleaning, a 2 nm Ti adhesion layer and a 50 nm Au seed layer are deposited by thermal evaporation. This layer serves as the cathode. (b) The chip is spin coated with a 6.5 μm thick layer of photoresist and subsequently patterned by optical lithography (c+d). The resist structures should be slightly taller than the desired thickness of the wires. In our example, a positive tone resist with high pattern stability in acidic and alkaline plating baths is used.

In the following electroplating step (e), the chip and a Ti/Pt mesh anode are connected to a power supply and submerged in 1 liter of electro-

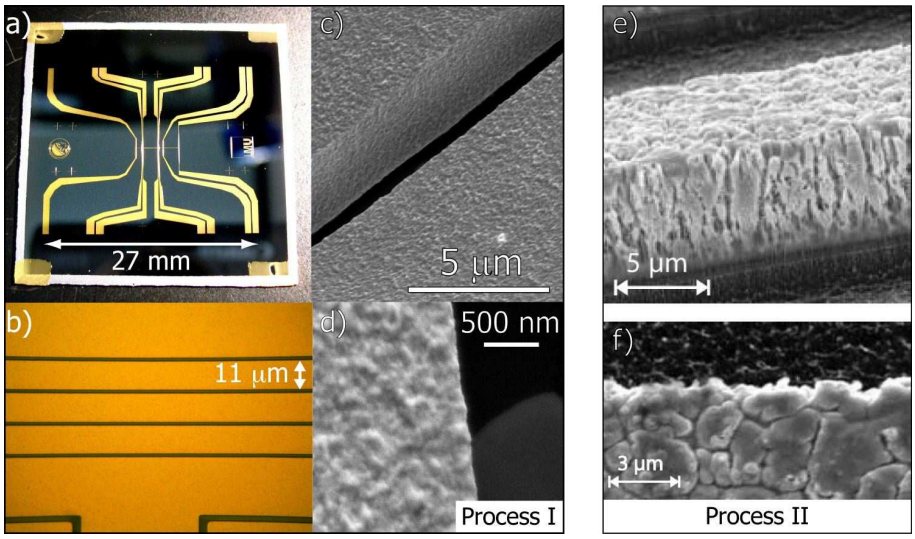

Fig. 1.3 Electroplated gold wires fabricated with two different processes. (a)-(d) Wires of 5 μm thickness on a Si chip, fabricated with the process of [41]. (a) Entire chip with contact pads. (b) Close-up of (a). The gaps between wires are 3 μm wide. (c)+(d) SEM pictures of the wires. The grain size of the gold is 200 nm, the r.m.s. surface roughness is 15 nm. (e)+(f) For comparison, SEM pictures of wires fabricated with the process of [42] are shown (thickness 4.5 μm). Grains of micrometer size are visible, the r.m.s. roughness is 200 nm.

plating solution, whose temperature is carefully controlled in a water bath. In our example, a solution from Metakem is employed, which is based on ammoniumsulfite-gold(I) ($[(NH_4)_3Au(SO_3)_2]$). It is commonly used for dentistry and jewelery and yields very smooth gold deposits of 99.99% purity. To deposit gold, the desired plating current I is driven through the electrolytic cell. Stirring helps to avoid local depletion of the solution and thus ensures a more homogeneous gold layer. The thickness h of the gold layer deposited after a time t can be determined by Faraday's law: $h = \alpha \frac{ItM}{nFS\varrho} = 1.1 \times 10^{-10} \frac{\mathrm{m}^3}{\mathrm{A\,s}} \times \frac{It}{S}$, where M the molar mass and ϱ the mass density of gold, F is Faraday's constant, $n = 1$ is the charge of the gold ions, and $\alpha \approx 1$ the current efficiency for gold plating. The surface area S of the deposited gold film is given by the surface area of the wire layout plus the contact pads and connectors. In the parallel plate configuration, the current density is approximately constant over the exposed gold areas of the chip. (f) After the wires are electroplated to the desired thickness, the resist is stripped. In the final step (g), the Au seed layer and the Ti adhesion layer are removed by a wet etch with aqua regia. This isolates the electroplated wires from each other. The gold etch also attacks the wires, increasing surface roughness. It is therefore

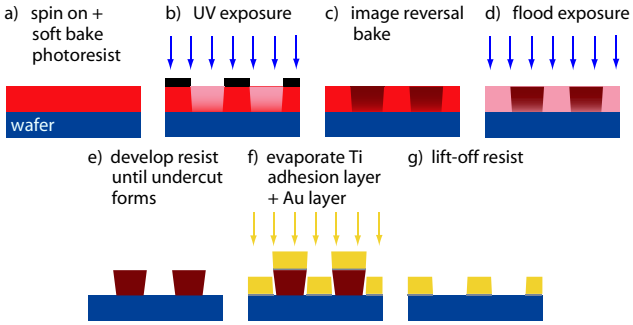

Fig. 1.4 Lift-off sequence with an image reversal resist. Gold is deposited by e-beam evaporation. The process steps are explained in the text.

desirable to work with a seed layer as thin as possible. Figs. 1.3(a)-(d) show electroplated gold structures on Si chips fabricated with this process.

The quality of the electroplated wires crucially depends on the choice of the plating solution and on the process parameters. Different solutions (and also the same solution at different process parameters) deposit gold of very different grain size [38]. Moreover, the complex bath chemistry can be disturbed by contaminants. Some processes result in deposits with micrometer grain size [42], resulting in inhomogeneous current flow in the wires and thus roughness of the generated potentials. Optimized electroplating processes, however, result in structures with very low roughness [39,41]. In Fig. 1.3(c)-(f), SEM pictures of electroplated gold wires fabricated with the processes of [41] and [42] are shown in comparison. The roughness of the wires of [41] is about one order of magnitude smaller than that of [42].

1.5.1.2 Evaporation and lift-off metallization

Evaporation and lift-off metallization is a standard technique for fabricating metal structures of high quality [35]. In this technique, patterned resist acts as a mask for evaporated gold. After removal of the resist ("lift-off"), only the desired gold structures remain on the chip. Gold layers deposited by thermal or electron-beam evaporation often have smaller surface roughness than electroplated wires. This is important for generating smooth trapping potentials for waveguides or 1d traps [43] and for using the wire layer simultaneously as a mirror [44] for a mirror-MOT [36]. Evaporation allows very precise control over the thickness of the deposited material. However, the thickness is limited by the slow deposition rate and substantial material consumption to a few μm at maximum. An alternative for thicker structures is sputtering of the metal, or electroplating (see previous section). Evaporation and lift-off was adapted to atom chip fabrication as described in [5, 23, 40, 41, 45].

An example of a lift-off sequence is illustrated in Fig. 1.4 (a detailed recipe can be found in [41]). (a) The substrate is spin-coated with a 1.6 μm thick layer of photoresist. An image reversal resist is used, which allows one to create resist sidewalls with a negative slope ("undercut"), which is crucial for lift-off metallization. (b) The resist is exposed for a few seconds with UV light through a mask which bears a negative image of the wires to be fabricated. Due to the small exposure dose, the resist is not fully exposed down to the substrate. This leads to the negative slope of the resist sidewalls after image reversal and development. (c) An image reversal bake on a hot plate at a carefully controlled temperature cross-links the resist in the exposed areas and thus renders it insoluble in the developer and insensitive to further exposure. (d) Subsequently, the chip is flooded with UV light, which now renders the previously unexposed areas soluble. (e) These areas are removed during development. The development time is carefully adjusted to control the formation of the undercut. Residues of photoresist are removed by a short oxygen plasma cleaning step. Subsequent baking of the resist structures on a hot plate improves resist stability. (f) A 1 μm thick layer of gold is deposited on top of a 3 nm thick Ti adhesion layer by e-beam evaporation in a UHV evaporation chamber. The resist acts as a mask for the gold, while the undercut prevents gold in the resist trenches from sticking to gold on top of the resist. (g) Lift-off is performed in a bath of hot acetone. This removes the resist and the gold on top of it and leaves behind the desired structures. If necessary, lift-off can be forced by agitation or by mild ultrasound.

For successful lift-off, the resist layer should be somewhat thicker than the thickness of the deposited gold layer. The resist undercut can be adjusted by changing exposure time, image-reversal temperature, and development time. A strong undercut can be seen in an optical microscope as a bright outline of the resist edges. However, for very small periodic structures, mechanical and thermal stability of the resist requires that development be stopped before the bright outline is visible. For process optimization, the undercut can be observed with an electron microscope, see Fig. 1.5.

Fig. 1.6 shows wires that were fabricated by evaporation and lift-off [5, 41]. The surface and edge roughness of the wires is small, resulting in very smooth magnetic potentials. Moreover, the gold wire layer can serve as a high-quality mirror if the gaps between the wires are sufficiently narrow.

1.5.1.3 **Wet and dry etching**

The simplest subtractive technique is wet etching, which is illustrated in Fig. 1.1 above. After the resist has been patterned, the chip is submerged and agitated in a suitable etchant (aqua regia in the case of gold wires), which removes the metal layer in the areas not covered by the resist. Wet etching results in relatively rough wire edges. Moreover, the metal is removed isotropi-

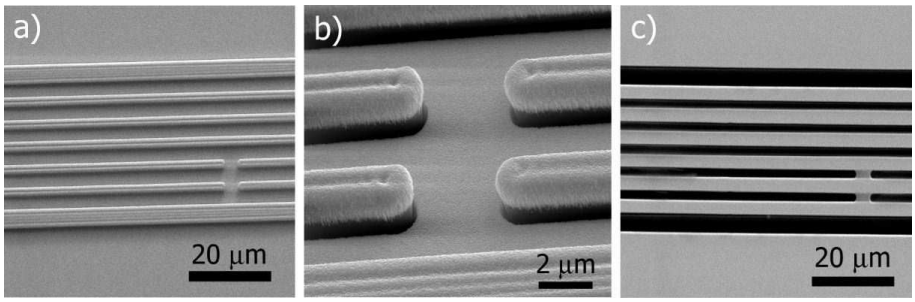

Fig. 1.5 SEM images of gold wires before and after lift-off. (a) Resist structure with deposited gold on top. (b) Close-up of (a), the undercut of the resist sidewalls is visible. (c) Gold wires remaining after lift-off.

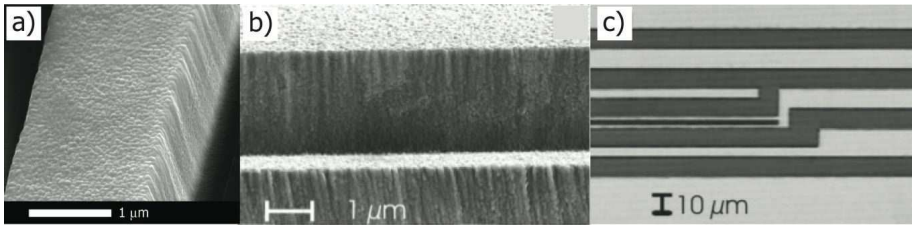

Fig. 1.6 SEM images of micrometer-size atom chip wires fabricated by evaporation and lift-off. (a) Gold wire, $1\ \mu$m thick and $1.7\ \mu$m wide [41]. The grain size of the gold is ~ 100 nm, the r.m.s. surface roughness is 3 nm. (b)+(c) Gold wires of [5] with $50 - 80$ nm grain size.

cally, and wet etching is thus not suitable for fabricating structures with steep side walls and high aspect ratio. By contrast, some dry etching techniques such as reactive ion etching [35] are very anisotropic, and can thus be used to fabricate high aspect ratio structures with steep edges. Brute force ion etching (called ion beam milling) may also be used if a thin layer of metal needs to be etched and the lift-off method is not feasible, for example, when high evaporation temperatures are used (e.g. if one needs large grain size), and the resist may only be put after the evaporation process (this method has been used in [7]).

For wet and dry etching, it is essential to choose an etchant that effectively removes the material to be patterned, but leaves intact additional structures on the chip and the functionality of the etch mask. The etch mask does not have to be a resist structure, it can also be a suitable patterned metal or dielectric layer. Two very useful papers with hundreds of etch rates for a large number of materials in different wet and dry etches are Refs. [46, 47]. They are also useful for choosing the right chemicals for cleaning and resist stripping tasks.

Besides etching, subtractive patterning techniques include focused ion beam milling (see the next section), which can be used to structure arbitrary

materials, and laser machining, which is useful e.g. for hole drilling. These techniques differ from etching in that they do not require a physical mask.

1.5.1.4 Designing potentials by post processing the wires

In general the magnetic potentials on atom chips are formed by the subtraction of two (large) magnetic fields, the field of a current carrying wire and a (homogeneous) bias field (see other chapters in this book). The value of the magnetic field at the potential minimum δB_{min} is determined by the angle between the field of the wire and the bias field. A small change of the current direction results in a significant change in the trapping potential. A deviation of the current flow by $\vartheta \sim 10^{-5}$ rad can lead to $\delta B_{min} \sim 1$ mG which corresponds to 67 nK for trapped Rb atoms.

One can implement slight changes in the current path deliberately by sculpturing the bulk of a lithographically patterned plane conductor [48] and thereby fine tune or even design local features in the trapping potential. The contributions of a current flow pattern with wave vector k to the magnetic field are exponentially damped with height z as e^{-kz} when receding from the wire. Therefore, in order to achieve a modulation of a fraction η_0 of the maximum achievable field at a minimum structure size $\lambda_{min} = 2\pi/k_{\max}$ one has to stay at distances of $z < -\frac{\log \eta_0}{k_{\max}}$ (for details see [48,49]).

This post processing of the chip structures can be done with a Focused Ion Beam (FIB) technique [50], which allows to create modifications with high precision (< 20 nm) and large aspect ratios (height/width > 30). The Heidelberg/Vienna group experimentally demonstrated the power of this technique by sculpturing a 10 μm wide and 2.5 μm thick gold conductor on a Si substrate [48,51] (Fig. 1.7).

1.5.2 Effects of roughness and homogeneity of the fabricated structures

A small change of the current direction results in a significant change in the trapping potential. Irregular current flow will result in uneven potentials with significant roughness.

After the first creation of a BEC on an atom chip a number of groups observed large roughness in the magnetic potentials holding the atoms. In many cases even a 1 μK *thermal* cold atom cloud was fragmented into many components when approaching distances below 100 μm from the wire [52–56]. This potential variation originates from inhomogeneous magnetic field components ΔB in the direction *parallel* to the current carrying wire [57] and can be attributed to variations in the current flow direction in the chip wires. Common to all but one of these experiments was, that they used electro plated wires to hold the trapping currents (the experiment by the Sussex/Imperial

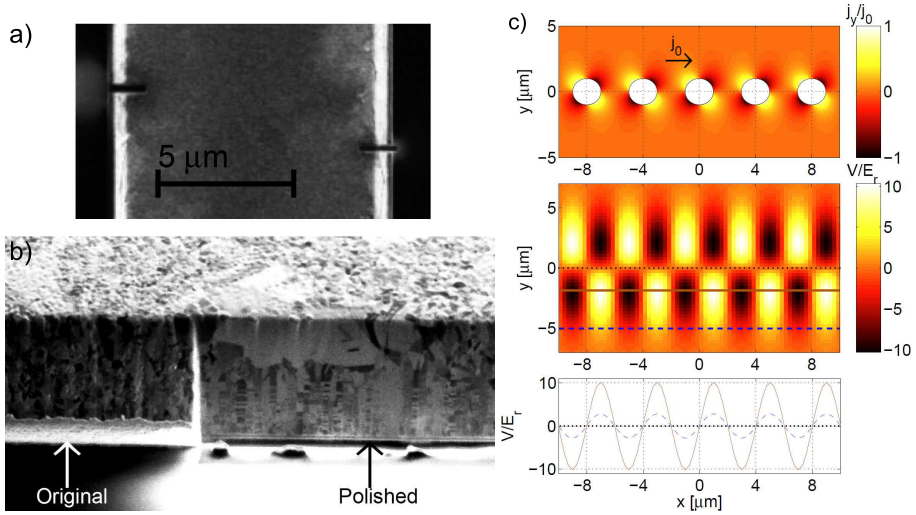

Fig. 1.7 Examples of wires sculptured by FIB *a)* **Double well** created by making two 1 μm deep, 0.2 μm wide cuts in opposite edges of a trapping wire. *b)* **Polishing** the wire edge as imaged by the FIB itself. The polished region (on the right) is smoother and reveals details of the structure of the gold wire. The contrast in the image is given by the ion reflection coefficient, varying with the relative orientation of the crystal axes of the gold grains. The picture shows a small region of 9.2 μm $\times$ 5.1 μm at the end of the polished section. *c)* **Magnetic lattice** with periodicity a=4 μm created by a string of holes with diameter D=a/2 in a wire with thickness d=a/2 and width w=10 μm. *Top*: Current density j_y in the transverse direction. *Center*: The potential modulation V at a height of z=6 μm, scaled to the characteristic energy $E_r = \hbar^2 k_a^2 / 2m_{Rb}$ (lattice vector $k_a = 2\pi/a$). *Bottom*: The potential along the lines drawn in the central image. The maximum modulation with a peak-to-peak depth $V_0 \simeq 20\, E_r$, is obtained at y=2 μm (orange continuous curve) while $V_0 \simeq 6\, E_r$ for y=5 μm (blue dashed curve).

College group used a drawn copper wire [54]). In an experiment by the Orsay group, the large potential roughness observed was clearly identified as coming from the rough edges of the fabricated wires, and the model of Wang et al. [58] provided a full quantitative explanation [55, 56]. In many cases the observed modulations were so strong that they prevented the creation of a continuous elongated BEC.

At about the same time in 2003 it became clear that this is not the general case. Such strong potential roughness was not found in the experiments at Heidelberg [43, 59] using atom chips with gold wires evaporated on a Si substrate and structured by the lift-off technique [5]. Nevertheless, a very small potential roughness remains which is also magnetic in origin. Measurements of the potential landscape over the whole width of a 100 μm wide wire, by scanning the position of the condensate across the wire using the BEC mag-

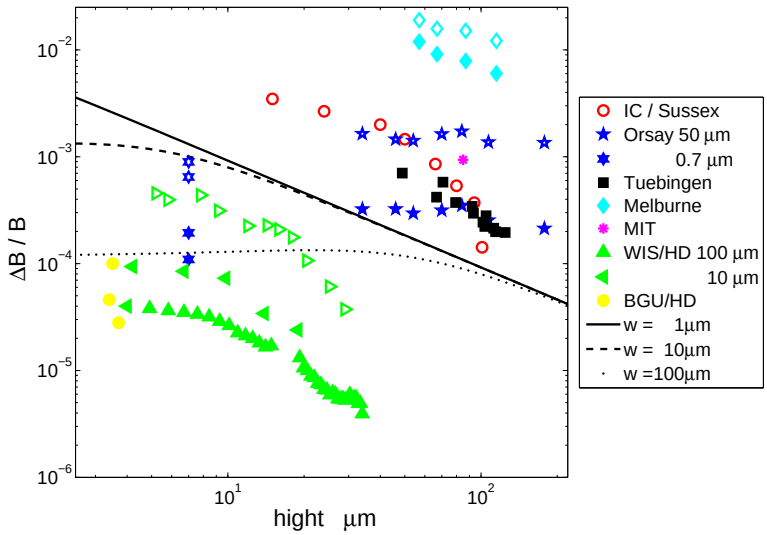

Fig. 1.8 Comparison of different atom chip potential roughness measurements. Data is taken from figures in the published literature and PhD theses and displayed with color codes according to the experimental group. Filled symbols denote *rms* values, and data displayed as open symbols are peak to valley maximum height of the roughness. *Sussex*: data from a gold coated copper wire [61]; *Orsay*: data from an electro plated wire [55, 56], and recent data from a 5 wire setup on an evaporated gold chip; *Tübingen*: data from electroplated wires (PhD thesis, J. Fortagh); *Melbourne*: data from a permanent magnet atom chip [13]; *MIT*: data from electro plated wires; *WIS/HD*: data from the analysis chips fabricated at the Weizmann Institute of Science: a 100 μm wire [43], 2003 data from various 10 μm wires [59, 62]. The open triangles give the peak to valley of the worst ever roughness observed in HD: a 10 μm wire (PhD thesis, L. Della Pietra). *BGU/HD*: Recent data from 3 different wires fabricated at Ben-Gurion and analyzed in HD [7].

netic field microscope [6,60], show no significant increase near the wire edges. A detailed analysis clearly showed that the edge roughness model can not explain the observed potential variations [43,59].

Even more surprising are the findings of Aigner et al [7] where the current flow in 3 different wires with different grain size and wire thickness was probed. The measurements showed that the thinnest wire with the largest grains had the smoothest current flow. A detailed analysis of the measured potential landscape and a comparison to the surface roughness of the gold layer clearly show that the local properties of the metal, and not imperfections in the wire boundary are the key to the current flow variations in the wires with the smoothest potentials [63].

It is interesting to compare the potential roughness observed on different chips and in different experiments. In most applications of atom chips an important parameter is how large the potential roughness ΔB is in comparison to the energy scale of the transverse confinement $\omega_\perp$. A stringent requirement for 1d experiments is $\hbar\omega_\perp \gg \mu\Delta B$, where $\mu = \mu_B g_F m_F$ is the magnetic moment of the trapped atomic state. The magnetic confinement $\omega_\perp \propto d^2B/dr^2$ is determined by the magnetic field gradient dB/dr and the longitudinal Ioffe field B_{Ioffe}. To achieve the same ratio $R_{\omega\perp} = \mu\Delta B/\hbar\omega_\perp$, the allowed relative magnetic field roughness for a trap built at height h above a flat wire of finite width w scales like:

$$\frac{\Delta B}{B} < R_{\omega\perp}\frac{2w}{(w^2+4h^2)(\frac{\pi}{2}-\arctan[\frac{2h}{w}])}\sqrt{\frac{\mu_B g_F m_F}{MB_{ip}}} \tag{1.1}$$

Fig. 1.8 shows a comparison of a large variety of measured potential roughness data from many different laboratories.

1.5.3 Special metals

1.5.3.1 Alloys

One of the high priority goals in atom chip research is the increase of lifetime and coherence time for ultracold atoms trapped in magnetic potentials close to the surface. This is important for both scientific aims and technological applications. Progress towards this goal demands the control and reduction of magnetic noise produced by the metallic components of the atom chip. Randomly fluctuating magnetic fields are generated by thermal current noise in the conducting chip elements and reduce the number of trapped atoms (losses), increase their temperature (heating) and lead to a phase uncertainty in the atom's state (decoherence) - see, for example, [64] and references therein. Theoretical analysis of the magnetic noise generated by a normal metal [65–68] predicts a fast reduction of the lifetime τ with the decrease of the distance z_t between the trapped atom and the metal surface (trap height); this is in excellent agreement with lifetime measurements [61, 69, 70]. At a trap height less than $10 \div 20\,\mu$m, thermal magnetic noise may exceed all other harmful influences on the atom cloud (technical noise due to the current supply instability, residual gas collisions, stray magnetic fields) and could present the dominant limit for the lifetime.

As is well known by now following the work of Carsten Henkel (see the corresponding chapter in this book), cooling of normal metals such as gold or copper will not reduce the harmful effect of thermally induced noise on the atoms. Hindering processes such as spin-flip (reducing trap lifetime), heating

and decoherence will thus not be suppressed by cooling the atom chip. The reason for this rather counter intuitive behavior has to do with the fact that the strength of the relevant magnetic noise is proportional to $R = T/\rho$ where T is the metal surface temperature and ρ its resistivity. As ρ is typically linearly dependent on T (due to phonon scattering) R does not become smaller with dropping temperatures and typically even becomes larger. As presented in the next section, superconductors are expected to have much smaller noise, but on the other hand present other challenges such as sensitivity to external magnetic fields and inhomogeneous current distribution. The question therefore arises if one may find a material where on the one hand cold temperatures do lower the level of R and on the other, a simple material is used.

Indeed alloys have such features. On the one hand they are a simple metal easily deposited (e.g. with sputter), with no sensitivity to external magnetic fields and with an homogeneous current distribution, and on the other their R drops with dropping temperatures. The reason for this behavior lies in the special dependency of ρ on T in alloys. At low temperatures, resistivity due to imperfections and impurities, if large enough, may become dominant over that dependent on phonon scattering. Alloys have impurities and hence the resistance becomes a constant at low temperatures. This is explained in detail in Ref. [71], which also presents the data for numerous metals. As an example of the benefits of such a material, we present in Fig. 1.9 how the spin flip rate behaves as a function of distance to the surface. The fact that such a simple choice of material may make a difference of up to two orders of magnitude in the lifetime, shows clearly the important role material engineering can play in atom chips.

1.5.3.2 **Superconductors**

In the last few years, the application of superconducting materials to atom chips has been widely discussed as a perspective to extend the lifetime of cold atoms [68,73–76]. A recent theoretical estimate [75] of the magnetic noise caused by a superconductor in the Meissner state showed that the lifetime of atoms trapped above a superconducting layer would be, at least, six orders of magnitude longer than above a normal metal in the same geometry. The analysis presented in [76] predicts an atom lifetime of 5000 s at a trap height of 1 μm. For comparison, at the same height in a normal metal trap the lifetime is less than 0.1 s [70].

Details of experiments with superconductors may be found in **??**. Here we give a brief account with emphasis on fabrication. Two first realizations of atom chips with superconducting elements have been reported in Refs. [77,78] and [79]. In both setups, the trapped atoms were ^{87}Rb. In the Paris experiment, the current-carrying wires (in “U" and “Z" shape) were made of niobium and operated at about 4.2 K. The obtained atom spin relaxation time τ_s

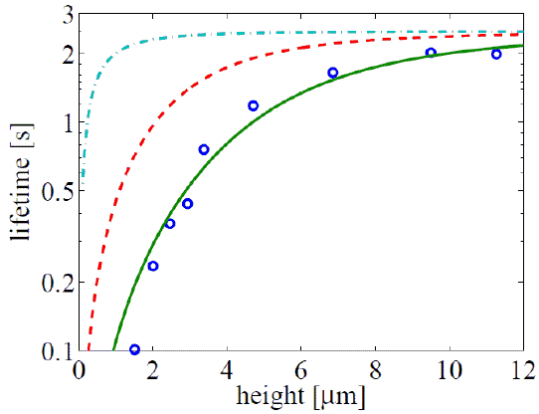

Fig. 1.9 Comparison of trapping lifetimes of ^{87}Rb atoms above a copper wire on an atom chip [70] with a theoretical calculation (solid line) - taken from [71]. Predicted lifetimes are also shown for a similar wire made of an alloy of Ag with 5.5% Au content, cooled down to T =77 K (dashed) and 4.2 K (dash-dotted). Note that the calculation in [71] differs from the one made in [70]. Van der Waals forces are not taken into account. Let us also mention that the maximum noise reduction factor of 75 is not visible, due to the affect of the technical noise and/or background gas collisions limiting the lifetime in this experiment to a maximum of $\tau_{\text{tech}} = 2.5\,s$ [72].

was estimated as 115 s. This value is comparable to the best one achieved for atoms trapped near normal-metal wires [80]. In the second experiment [79], special efforts have been undertaken to reduce the influence of technical noise. Utilizing a MgB_2 film, a "Z"-shaped wire was fabricated as a part of a closed superconducting loop and operated in the persistent current regime. This permits to disconnect the current supply and get rid of its instability i.e. technical noise. To our knowledge, in both experiments the trap lifetimes were limited by processes other than the magnetic noise generated by the superconducting elements of the atom chip. Furthermore, to the best of our knowledge, to date no atoms were taken in these two experiments to a distance below a few tens of μm from the surface.

The Paris atom chip was made on a 65 mm x 30 mm silicon wafer (thickness 360 μm) with a 500 nm insulating oxidized layer. It was coated by a 900 nm thick layer of Nb by cathodic plasma sputtering. A "U"-wire (width 280 μm) is used for the on-chip mirror-MOT, and a "Z"-wire (width 40 μm) for the magnetic Ioffe-Pritchard trap. The cross section of the "Z" wire was 40 x 0.9 μm^2. The wires and contact pads are produced by standard optical lithography with a laser-printed mask followed by reactive ion etching. The resulting wire edge precision is about 5 μm. A gold layer of thickness 200 nm was deposited on the niobium wire to increase its reflection. The current through the

"Z" wire reached 1.5 A, close to the critical current value of 1.94 A. The critical current density obtained for the niobium wire was $J_c \approx 5 \times 10^6$ A/cm^2 at 4.2 K.

In the Japanese group, a magnesium diboride MgB_2 film of 1.6 μm thickness was grown by molecular-beam epitaxy (MBE) on a sapphire C substrate (10 x 10 x 0.5 mm). The cross section of the "Z"-wire was 100 x 1.6 μm^2. The persistent superconducting current of $I = 2.4$ A in a "Z"-structure was significantly lower than the critical value of $I_c \approx 16$ A (the critical current density at 4.2 K is about $J_c \approx 10^7$ A/cm^2 and the transition temperature of MgB_2 is $T_c \approx 35$ K). The top of the MgB_2 thin film was coated with a thin gold layer to prevent radiation heating and for better reflection. The circuit pattern on the chip was produced by removing the unnecessary part of the MgB_2 thin film by ion milling. This group has also demonstrated trapping atoms on a Nb film [81].

Recently, two additional groups joined the experimental effort: In the Singapore group, an atomic interferometer was created on the basis of a high-T_c superconducting film [82, 83]. The $YBa_2Cu_3O_{7-\delta}$ (YBCO) film was grown by epitaxy on a yttria- stabilized zirconia (YSZ) single crystalline substrate. The lattice constants of YBCO and YSZ are matched, allowing homogeneous growth of the superconducting material. The final thickness of the YBCO film was 600-800 nm. On top of the YBCO film a 200 nm thick layer of gold was deposited to protect the superconducting material. Structuring of the chip is performed by two different techniques. These are standard optical lithography followed by a wet-chemical etching as well as direct femto-second (fs) laser ablation. The standard lithography procedure has a resolution limit of about 1μm for the structure size. With the fs-laser ablation procedure the desired patterns on the chip are realized by locally removing the gold and YBCO layers with focused laser pulses (2 μJ, 130 fs, center wavelength 800 nm), resulting in insulating regions between the superconducting structures. In this laser assisted structuring technique, it is crucial that the film is not heated. In case of heating, oxygen would be lost and the superconducting properties of the thin film would degrade. This requirement sets the demand for using fs-laser pulses and may at times set the wet etching as the preferable method. In the final chip, the roughness of the surface was almost negligible with an rms value of the surface height of only 2.3 nm. The critical current density J_c at liquid nitrogen temperature was 2 MA/cm^2. Recently, this group has managed to trap atoms in the field of a vortex [84].

In the Tübingen group [85], a cylindrical niobium wire of diameter 0.125 mm has been used. The wire was mechanically clamped to copper plates firmly attached to a helium cryostat. From the published data one may assume that the small distance of about 25-30 μm was achieved between the atoms and the super current (where one has to take into account the super current radius for each temperature).

Aside from low thermal magnetic noise, the application of superconductors in atom chips may be advantageous also due to high current densities without Joule heating, and practically zero electric fields across the superconducting elements. In addition, as noted, technical noise can be reduced by inducing a persistent current. Hence there is significant motivation to make available simple fabrication procedures for superconductors. Recently, two works have analyzed in detail the trapping parameters of cold atoms in magnetic traps made by type I and type II superconductors [86, 87].

1.5.3.3 Semiconductors

In the future, atom chips might be built like integrated circuits from a single semiconductor substrate. For example, the current used for trapping and manipulating atoms will flow in an epitaxially grown layer, that is covered by an insulating layer on top. Such an approach has the advantage that the epitaxially grown material is more uniform and better controlled than the wires deposited onto the surface. In addition, such a structured semiconductor atom trap may be used to probe the current flow in the semiconductor, by using the cold atoms as a magnetic field microscope [6, 7, 60].

First steps to develop a semiconductor based atom chip were carried out by the Heidelberg/Weizmann team [34]. The chips were fabricated from a GaAs wafer grown using molecular beam epitaxy (MBE) at the Weizmann Institute of Science. Such a chip contains a super lattice of twenty layers of GaAs and AlGaAs which are used as an etch stop layer for selective etching. On top of it, about one micron of Si doped (n+) GaAs is grown as a conductive layer. The measured 3d charge carrier density is $N \sim 6.4 \times 10^{18}$, the mobility is $\mu = 1160$ cm^2/V sec, and the 2d resistivity of this layer is 8.5 Ω

The wire structures are then fabricated into the GaAs wafer by UV lithography and dry etched by reactive ion etching, which is stopped when the super lattice below the doped layer is reached. The etch results in straight walls. In the patterned semiconductor wires the charge carriers are located in the doped layer below the surface, which is insulating. They are contacted by alloying: Several metal films are evaporated in defined order and thickness (50 Å Ni, 400 Å Ge, 800 Å Au, 200 Å Ni and 2000 Å Au) onto the regions, where the semiconductor is going to be contacted. The first 4 layers are to be alloyed into the surface and contact the semiconductor, the top gold layer supports enough metal to allow bonding. Alloying is accomplished by a well defined thermal cycle heating the sample up to 430°C [34].

Finally the small GaAs chip is mounted on a standard gold layer carrier atom chip by gluing, and contacted by wire bonding. The atoms are to be trapped and cooled on the carrier atom chip, and then transported to the semiconductor chip. Pictures from a fabricated and mounted chip can be seen in Fig. 1.10.

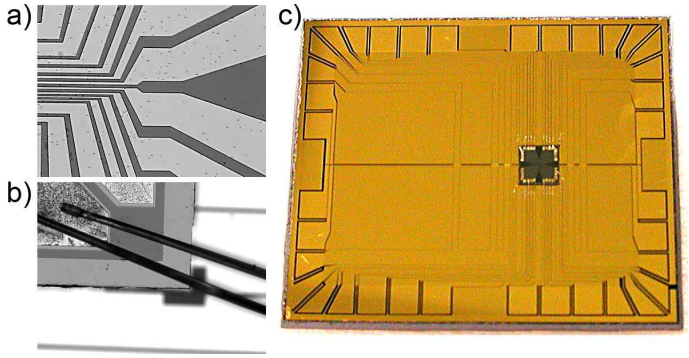

Fig. 1.10 Example of an atom chip fabricated in a GaAs substrate. *a)* Central region of the chip. The deep etched trenches defining where the doped layer is removed are shown dark *b)* Wire bonds connected to the alloyed metal pads on the GaAs chip *c)* Overview of the GaAs chip mounted on a carrier chip.

1.5.4 Permanent magnets

Most atom chips rely on a pattern of current-carrying wires to generate the necessary magnetic fields. By contrast, it is also possible to use patterned films of permanently magnetized material for this purpose (see chapter **??**). The ideal magnetic material for use in atom chips has a large remanent magnetization and coercivity, regardless of the shape, is very homogeneous, has a high Curie temperature, is corrosion resistant, and UHV compatible. Several groups have developed fabrication processes for permanent magnet atom chips, see e.g. [10, 11, 88–95] and references therein, and we discuss a few examples in the following.

Commercial magnetic storage media such as videotape or hard disks provide a convenient way to prepare small magnetic structures. In [88] an atom mirror was fabricated by etching of a common hard drive. The hard drive provides a large area of thin magnetic film whose remnant magnetic field and coercivity can be as large as 7 and 3 kG, respectively. The atom mirror is fabricated by etching 2 μm wide, 100 nm deep trenches into the film. Standard photolithography is used to create the etch mask. The cobalt alloy of the magnetic film is granular, which enhances the coercivity and allows one to magnetize the material in plane and parallel to the short axis of the magnetic strips.

In [89] it was demonstrated that a pattern of magnetization recorded in commercial videotape can be used to generate an array of elongated magnetic microtraps. Videotape can store patterns with feature sizes down to a few micrometers using simple commercial recording equipment adapted in the laboratory. It is designed to hold data reliably for long periods of time and has a high coercivity (1500 Oe), making the magnetization insensitive to

the presence of magnetic bias fields. The tape used in [89] has a 3.5 μm thick magnetic layer containing iron-composite needles, 100 nm long with 10 nm radius, which are set in a glue and aligned in parallel. The film is supported by a polymer ribbon 11 μm thick. Remarkably, the tape is UHV compatible and is able to withstand baking at 120°CṪhe same group has also investigated various other permanent magnetic materials for atom chips, such as magneto-optically patterned CoPt thin films [90].

The Amsterdam group has found that FePt is a magnetic material ideally suited for the use in atom chips [10, 91–93]. Their first chip was made out of a 40 μm thick foil of FePt [10]. An "F"-like shape was cut out by spark erosion and glued onto a mirror. This produces a self-biasing Ioffe-Pritchard trap. The second generation atom chip uses structures lithographically written into a FePt film [92]. Fig. 1.11a shows a two-dimensional FePt pattern with the magnetization oriented perpendicular to the film, which has been used to create a large two-dimensional array of magnetic microtraps [12]. The 300 nm thick FePt film is grown in the ordered face-centered-tetragonal (fct) phase, which is magnetically hard with high uniaxial anisotropy constant. The measured remanent magnetization is $M_r = 670$ kA/m, the remanent to saturation magnetization ratio $M_r/M_s = 0.93$, and the coercivity $H_c = 0.95$ T. After baking for 3 h at 150°C in air, the magnetization had reduced by only 3%, and the film was found to be stable against typical time-varying fields applied in the experiment. The film is patterned using optical lithography and argon plasma etching. After patterning, the film is coated with a 100 nm reflective gold overlayer and magnetized in a 5 T magnetic field.

The Melbourne group uses atom chips based on perpendicularly magnetized multilayered TbGdFeCo/Cr films [11, 94, 95]. These films have a large perpendicular magnetic anisotropy and are suitable for the production of periodically grooved, micron-scale structures. Fig. 1.11b shows an example of a patterned film that can be used to produce a one-dimensional magnetic lattice. To pattern such magnetic films, a periodically grooved structure is first fabricated into a Si substrate by reactive ion etching. The TbGdFeCo film is then deposited on this grooved structure by magnetron sputtering. Because the magnetic anisotropy is found to deteriorate for a film thickness above 250 nm, a multi-layer structure is deposited, consisting of several layers of TbGdFeCo (160 nm) and Cr (100 nm) to achieve a total thickness of about 1 μm. A 10 nm Cr film and finally a 150 nm gold film are deposited on top of this structure in order to produce a mirror for the mirror-MOT. Measurements show that the remanent magnetization of the film is about 3 kG and the coercivity is about 6 kOe [95].

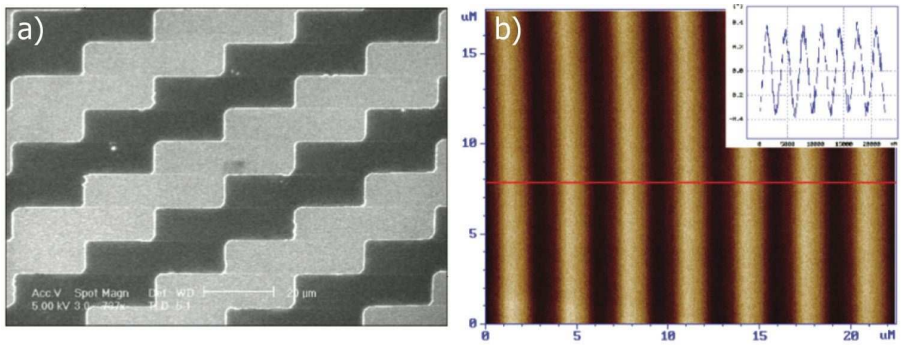

Fig. 1.11 Permanent magnet atom chips. (a) SEM image of the patterned magnetic film of [92]. The light gray areas correspond to the FePt pattern and the darker regions are the Si substrate. The film can be used to create a two-dimensional magnetic lattice potential. (b) Magnetic force micrograph of the patterned magnetic film of [94]. The structure is a 150 nm thick $Gd_{10}Tb_6Fe_{80}Co_4$ film on a 140 nm thick Cr underlayer on a Si grating structure with a period of 3 μm. The grooves are represented by the light regions and the inset shows a cross-section of the MFM signal along the indicated line.

1.5.5 Metal outlook

As the fabrication of magnetic field based atom chips evolves in the future, one would also need to look at additional forms of materials. Aside from the above mentioned metals, alloys, superconductors, semi conductors and permanent magnets, it stands to reason that additional classes of new materials will be investigated in the near future. Here, as an example, we shall focus on nano wires, molecules and metallic crystals, which are already being studied in several groups.

Nano wires (Fig. 1.12) constitute an interesting system. While the current may be sufficiently high to maintain magnetic traps, the Johnson noise may be sufficiently low to enable long spin flip lifetimes at small atom-surface distances. Lifetimes of seconds may be reached for atom-surface distances of less than one micrometer [49]. Fabricating nano wires may only be done through direct e-beam writing, and even then, requires considerable attention to details such as edge roughness and contact resistivities. We note that due to surface scattering, the nano wire resistivity may be high, an issue which may be solved by using crystalline nano wires, namely molecules, which are our next topic.

Molecules may form interesting conductors for numerous reasons. First, they may be able to sustain extremely high current densities. Second, they may suppress hindering effects such as Van der Waals and Casimir-Polder (CP) forces, corrugations due to imperfections causing electron scattering, and

noise giving rise to spin flips, heating and decoherence. Third, molecules have a relatively sharp absorption spectrum and hence may be put much closer to sensitive optical devices in comparison with normal metal wires. Finally, one may also look into a future in which molecules will self assemble into circuits (forming molecular electronics), and similarly may be used to assemble current carrying atom chip circuits.

A specific molecule that has recently attracted attention is the Carbon Nano Tube (CNT). The CNT may hold current densities of up to 10^9 A/cm^2 (two orders of magnitude higher than normal metals), may have ballistic transport (hence negligible scattering causing corrugations) and is also expected to produce less noise and CP forces. Two articles describe the advantages of CNTs [96, 97]. To the best of our knowledge, to date, no atoms have been trapped in the magnetic field of a CNT but several groups, such as the Tübingen group, are pursuing this goal.

CNTs come in different shapes and forms: from single-wall CNTs to multi-wall CNTs, from semi-conducting to metallic, and from suspended to substrate based. While a multi-wall CNT offers more current, it is also less crystalline in nature. While a suspended CNT offers less CP it probably also enables less current density due to the lack of a heat sink. It is unclear what the ultimate current limit of single wall CNTs is but while 20 μA seem to be enough for trapping at a height of a few hundred nanometers (also taking into account the CP force) [98], experiments at the Ben-Gurion University group show that CNTs of a few μm length are able to carry up to 50 μA.

Typically a Chemical Vapor Deposition sample will contain many CNTs with random orientations, lengths, and degrees of straightness. A preliminary survey is taken by AFM and, if suitable CNTs are seen, grids of Ti alignment marks (e.g. 2 μm long, 1 μm wide, 40 nm thick, 10 μm spacing) are grown by e-beam lithography (PMMA resist baked at 200°C) and thermal evaporation over several small areas of the Si wafer. After lift-off with NMP at 80°C these areas are then carefully scanned by AFM; co-ordinates for suitable CNTs are measured with respect to the Ti alignment marks.

The next step is to contact both ends of the CNT with parallel leads in order to form the "Z" shape typically used for Ioffe-Pritchard atom chip micro-traps (and now for CNT-based nano-traps). Pd leads are usually thought to have the best contact resistance to CNTs and are made by using a second e-beam lithography step with PMMA (the same as before) and are typically 30-40 nm thick and 1 μm wide, (see Fig. 1.12).

In the future, it is expected that CNTs will be grown in a controlled way along pre-defined paths. One such method, includes growth of CNTs along atomic steps in the substrate [99, 100]. An alternative method for controlling the CNT position and orientation utilizes an imprint process [101]. In such a case where the CNT's position and direction is determined by the user, one

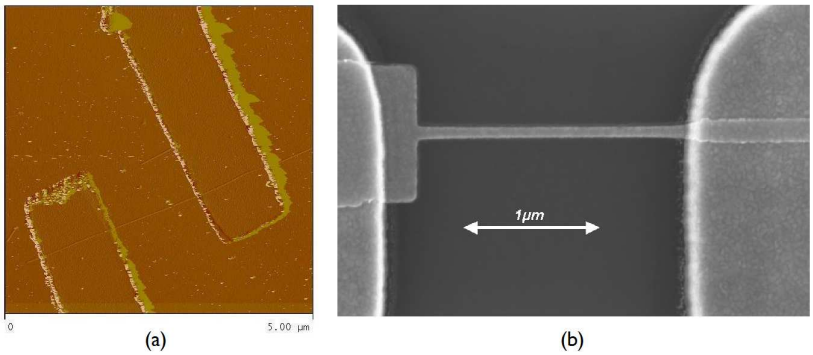

Fig. 1.12 (a) An AFM scan of a single wall carbon nano tube (2μm long connected to Pd pads [98]. Around 40μA were pushed through this CNT. (b) Nano wire: 50nm wide and 20nm thick [49] (fabrication of both samples done at the Ben-Gurion University fabrication facility).

may also etch the substrate before depositing the CNT, evaporate or electroplate a loading wire into the etched channel, deposit an insulating layer and obtain a smooth substrate by Chemical Mechanical Polishing (CMP) or other planarization methods described in this chapter, and then place the CNT on top - hence obtaining a truly monolithic CNT atom chip.

Before moving on, let us note that nano wires and molecules such as CNTs may be used also for other purposes. For example, ideas have emerged where plasmonic waves on such elements may be used to trap and couple light between nearby atoms. Another example, which was realized experimentally, includes utilizing CNTs for high efficiency atom counting. The experiment was conducted in the Tübingen group of J. Fortagh [102]. In Fig. 1.13 we show the CNTs used to create a high electric field for the purpose of ionization and ion counting.

Another class of materials that has so far not been used in atom chips is crystalline metals. There may be several advantages for utilizing such materials. To start with, they may offer reduced electron scattering and thus produce potentials with less corrugation. They may also be used in their electrically anisotropic form to significantly reduce decoherence even at room temperature (Fig. 1.14) [103].

Fabrication of atom chips using these materials is not trivial. To start with, these materials may not be deposited through evaporation and need to be grown in specialized methods. Typically, one can buy layers of these materials after which they will need to be bonded to a substrate (as they usually come as thick leafs or attached to dissolvable substrates), thinned (without causing too much surface roughness) and patterned. Obviously, standard lift-off may not be used here as the photoresist may only be put on top of the material.

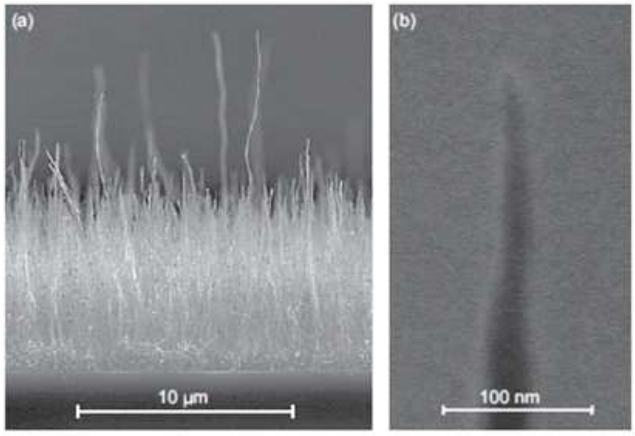

Fig. 1.13 Vertical CNTs used to create a high electric field for ionization of neutral atoms. The ions are then detected with single atom precision.

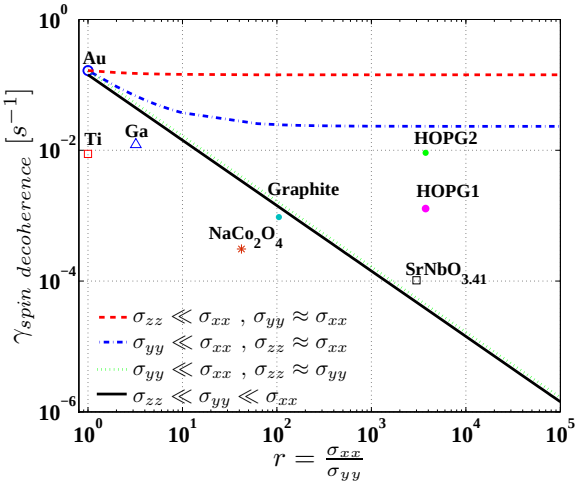

Fig. 1.14 The spin decoherence rate as a function of the electrical anisotropicity of the material [103]. The different lines represent different types of anisotropic materials (see legend). Several material examples are also shown.

Shadow masks followed by wet etching, ion beam milling or plasma etching will need to be utilized. In addition to the above, one would also have to utilize normal evaporated metals to make electrical contacts as the above crystalline materials may not have suitable conductivity in all directions.

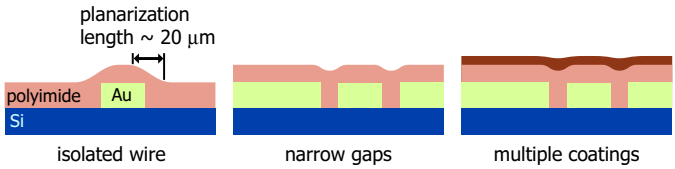

Fig. 1.15 Planarization and insulation with polyimide. Narrow gaps are easier to planarize than broader, isolated features. Multiple coatings improve planarization [41].

1.6 Additional features

1.6.1 Planarization and insulation

Dielectric layers for planarization and electrical insulation are essential for the fabrication of multi-layer chips. Besides the dielectric and planarization properties, good heat conductivity, ultra-high vacuum compatibility, and chemical stability in subsequent processing steps are important criteria for the choice of suitable materials.

Spin-on polyimide has been used in the multi-layer atom chip designs of [23,41]. It provides good planarization, electrical insulation, and is UHV compatible. Moreover, some polyimides can be directly structured by UV lithography. On the other hand, polyimide has a thermal conductivity which is about three orders of magnitude smaller than that of gold or silicon. Therefore, the polyimide layer has to be as thin as possible to allow for large current densities in the wires of the upper gold layer. To process polyimide, the chip is spin-coated with the polyamic ester. Subsequent curing of the polyimide is carried out at temperatures of typically 300-400°CḞully cured polyimide is resistant to solvents and most acids, but can be dry etched in an oxygen plasma [47].

As illustrated in Fig. 1.15, a layer of polyimide does not globally planarize a chip surface with an uneven topography. It rather acts as a "low-pass filter" which locally smoothens out the topography. Only features with a lateral extension smaller than the planarization length, which is $\sim$ 20 μm for the polyimide used in [41], can be fully flattened out [104]. The degree of planarization is higher for several thin coatings compared with a single thick coating of equal total thickness. Fig. 1.16 shows AFM measurements of the polyimide surface topography above gold wire structures. Thin gaps (5 μm wide) between 5 μm thick wires are planarized to a step height of 300 nm with three layers of polyimide. If necessary, the thickness of the polyimide could be reduced by subsequent back-etching.

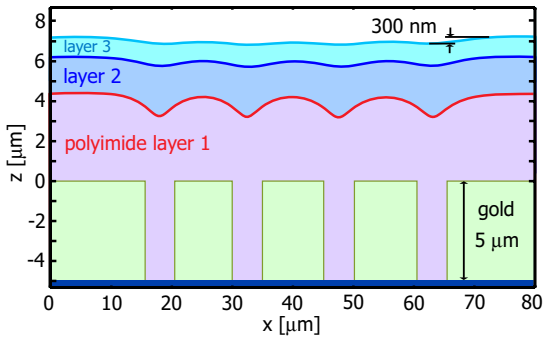

Fig. 1.16 Planarization results [41]. Surface topography of three polyimide layers above small gaps in a lower gold layer, measured with an AFM. Note the different scaling of the two axes. On this chip, the polyimide layers were 4.3, 1.9, and 1.0μm thick.

1.6.2 On-chip mirrors

It is often desirable to have a high-quality mirror as the uppermost layer on the atom chip. A mirror is required for the operation of a mirror-MOT [36]. Moreover, it enables imaging of the atoms very close to the chip surface, using an absorption imaging beam that is reflected from the surface [105]. The mirror can also be used for reflecting laser beams that generate optical dipole traps.

High-quality dielectric mirror coatings can be transferred to the chip using a replica technique [106, 107], which is illustrated in Fig. 1.17. In this technique, a detachable mirror coating supplied on a transfer substrate is glued onto the desired chip area using vacuum-compatible epoxy glue. The transfer substrate is manually removed, leaving the coating on the atom chip. Various types of dielectric coatings on transfer substrates are commercially available. By cutting the transfer substrate to the desired size, it is possible to only partially cover the atom chip with the mirror [29, 108]. The transfer technique can also be used for homogeneous metal layers [106]. The advantage compared to evaporating the metal layer is that pretty good planarization of underlying structures can be achieved.

Covering the uppermost wire layer with a dielectric mirror or metal mirror on a dielectric spacer is not always desired. The mirror layer increases the minimum distance of the atoms to the wires, thereby reducing the attainable field gradients. If the uppermost wire layer contains microwave guiding structures, the mirror changes the waveguide impedance and introduces additional losses or shields the atoms from the microwave field. In these cases, a viable option is to use the uppermost wire layer itself as a mirror [20, 44]. This requires high-quality metal deposits and narrow gaps between the wires.

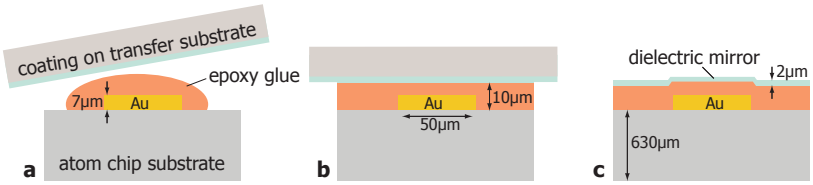

Fig. 1.17 Fabricating a dielectric mirror on the atom chip using the transfer technique [106, 107]. (a) A small drop of UHV-compatible epoxy glue is dispensed on the atom chip. (b) The transfer substrate with the dielectric coating is sandwiched onto the chip. (c) After curing the epoxy, the transfer substrate is lifted off, leaving the dielectric mirror on the atom chip. On a structured chip, epoxy shrinking causes small modulations of the mirror surface.

Experiments have shown that a mirror MOT is remarkably tolerant against the distortions of the light field caused by the gaps, even for gap sizes of the order of 10 μm. However, the gaps between wires cause clearly visible distortions on high-resolution absorption images taken with light reflected from the mirror.

Even if no dielectric mirror is desired, it can be advantageous to cover the uppermost metal layer on the chip by a few nanometers of a dielectric such as SiO_2. This prevents alkali atoms from contaminating the metal layer over time and degrading its reflectivity or even creating shortcuts between wires. A thin SiO_2 layer could also reduce the electric fields from alkali adsorbates on the surface.

1.6.3 Multi-layer chips

Many applications of atom chips in both fundamental science and technology require chips with complex multi-layer wire patterns. A multi-layer chip allows for much greater flexibility in trap design by avoiding wire crossings which would arise in a single layer. This is crucial e.g. for experiments on quantum information processing, which will eventually require large arrays of qubits in individually addressable microtraps on a single chip (see chapter **??**). Some proposals for quantum gates require the integration of microwave guiding structures on the chip in addition to the already complex DC wire structures [17,20]. Moreover, it is often necessary to combine wires of very different size and thickness on the same chip, e.g. because the experimental sequence starts with an ensemble of atoms in a large-volume trap, while the actual experiment is performed with a small Bose-Einstein condensate in a micrometer scale trap. In all these cases, multiple wire layers separated by dielectric insulation layers are beneficial. Here we discuss several examples

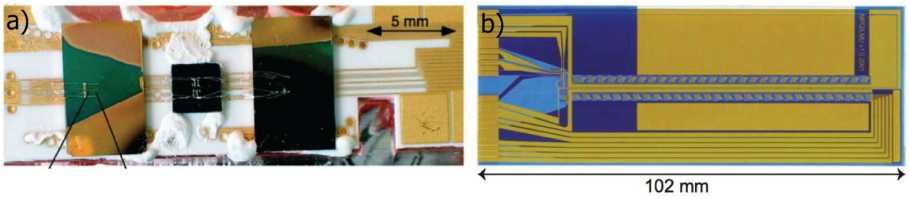

Fig. 1.18 (a) Atom chip of [22]. Three different experiment chips with micrometer size structures are glued on top of a carrier chip with larger structures for positioning of the atoms. (b) Atom chip of [108]. This magnetic conveyor belt is a two-layer structure with vias, fabricated by thick-film hybrid technology.

of multi-layer atom chips which have been used in experiments. A general introduction to multi-layer microfabrication is given in [104].

The simplest way to produce a "multi-layer" chip is to fabricate two single-layer chips and glue them on top of each other. This greatly simplifies fabrication because the processes used for the two layers are completely independent and the chips can be independently discarded if something goes wrong. This technique has been used e.g. in the experiments of [22], where a carrier chip with a standard layout of larger wires for initial trapping and transporting of atom clouds carries several experiment chips with dedicated micro- and nanostructures for the main experimental task, see Fig. 1.18a. The carrier chip used in [22] is itself a two-layer structure, with one wire layer on the front side and another one on the back side of the same substrate. For interconnecting the two layers, wire vias have to be fabricated through the 250 μm thick substrate. The vias are made by laser cutting of holes 400 μm in diameter and electroplating gold inside.

In [108], a two-layer chip is described in which the two wire layers are on the same side of the substrate, see Fig. 1.18b. The chip is fabricated using thick-film hybrid technology. This fabrication process is mainly employed in high-power electronics and is based on screen-printing with metallic and dielectric printing pastes. The desired structure is lithographically transferred to a fine-gauge printing mesh. The printing paste is then squeezed through this mesh onto the substrate. Large-format substrates and thick conductor layers with high current capability are standard with this technology. However, the structures are grainy and the minimum feature size as well as the thickness of the layers is of the order of tens of micrometers and thus not as small as in direct lithographic techniques.

While relatively simple to implement and useful in many cases, these techniques have two main drawbacks: there is a relatively large distance between the two wire layers and it is difficult to accurately align the structures on the different layers with respect to each other. To overcome these limitations, several groups have developed custom multi-layer chip fabrication

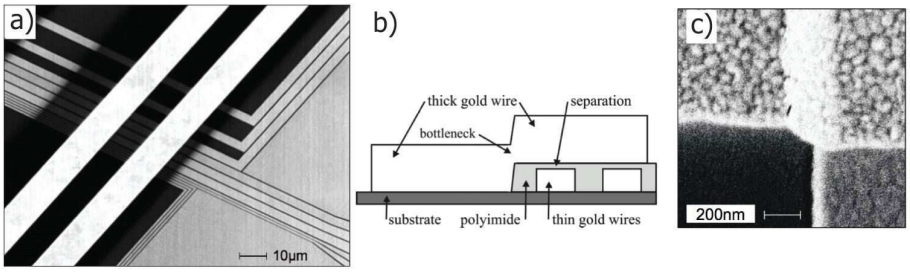

Fig. 1.19 Multi-layer atom chip of [23]. (a) SEM micrograph of the central part of the chip. $10\ \mu$m wide wires with a height of $1.4\ \mu$m cross structures created by e-beam lithography. The smallest features are 300 nm gaps between 700 nm wide and 140 nm high wires. Electrical insulation of the two layers is provided by 500 nm thick polyimide pads, visible as partially transparent layer. (b) Cross section of chip (not to scale). The step in the upper gold wire causes a bottleneck of reduced wire cross section. (c) SEM top view of the step. The wire runs from left to right in the upper half of the picture. In the lower right part the polyimide pad running from top to bottom is visible.

processes where the metal layers are fabricated by optical or electron beam lithography and separated by thin insulating layers of at most a few μm thickness [23,34,41]. This enables precisely aligned crossed wire configurations on a micrometer scale, greatly enhancing the flexibility in designing potentials for the atoms.

Fig. 1.19 shows pictures of the multi-layer chip described in [23]. It is fabricated using a combination of optical and electron-beam lithography, gold deposition by evaporation, and lift-off. On this chip, larger wire structures are fabricated on top of smaller ones, facilitating planarization of the lower layer. The two wire layers are separated by a polyimide layer, which is structured by optical lithography to cover only regions where conducting structures will cross. The insulation layer is thinned in an ozonator to about 500 nm and cured. This layer thickness proves to be sufficient to insulate the two conducting planes while providing good heat transfer and keeping the step height the top layer wires have to surmount to a minimum (see Fig. 1.19b-c).

Fig. 1.20 shows pictures of multi-layer chips described in [20,41]. The chips are fabricated using optical lithography. The chip shown in Fig. 1.20a-b has a lower wire layer of 5 μm thick electroplated gold, which is covered by three layers of spin-on polyimide with a total thickness of 6 μm. On top of the polyimide, a 1 μm thick gold wire layer is fabricated by evaporation and lift-off. On this chip, the small wires are on top of the larger ones. The three polyimide layers provide very good planarization. The smallest structures on the upper wire layer are several parallel wires of 2.5 μm width, separated by 2 μm gaps. Some of the wires on the upper layer form integrated microwave guiding structures. Fig. 1.20c shows a different chip, on which such a microwave

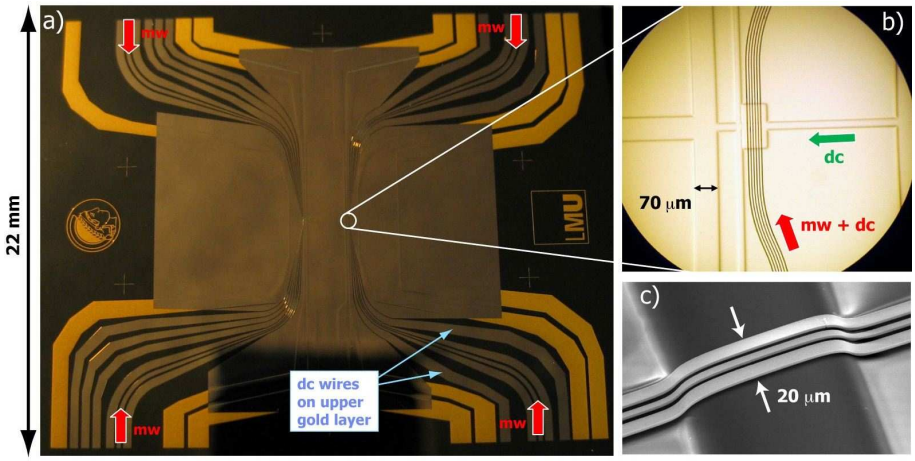

Fig. 1.20 Multi-layer atom chips of [20, 41]. (a) Photograph of a whole chip. Two gold wire layers are separated by a thin polyimide layer (see main text). Wires on the lower layer have an orange color because of the overlying polyimide. (b) Close-up of the central region of the chip. Parallel wires on the upper layer cross wires on the lower layer. (c) SEM micrograph of a different chip. Small gold wires (thickness 800 nm) forming a coplanar microwave guide cross a large transverse wire of 7 μm thickness. A single polyimide layer of only 4 μm thickness between the wires already provides sufficient smoothing of the step.

guide crosses a thick transverse wire on the lower gold layer, demonstrating the smoothing of the step by the polyimide.

1.7 Current densities and tests

An important parameter in all atom chips is the electric performance of the fabricated structures. Atom chips require current densities in the excess of $10^6 A/cm^2$ in continuous use. For a wire (height h and width w) to support such high current densities $j = I/wh$, the ohmic heat $P = RI^2$ created in the wires has to be efficiently transferred into the substrate and removed. The temperature rise and eventually the destruction limit of a wire depends not only on j and the length of the current pulse τ but also on the geometry and on material parameters like heat conductivity λ and heat capacity C_V. In a typical atom chip the wire is separated from the thermally conducting substrate by a thin electrical insulating layer which at the same time is a bad thermal conductor. This leads to two heat removal mechanisms on very different time scales [5].

The first process concerns the heat flow from the wire to the substrate through the insulating layer. In a 1d model, the timescale of this process is given by $\tau_{fast} = \frac{C_V h}{k - hj^2\rho}$ where k is the thermal conductance through the insulating layer and ρ the temperature dependent resistivity of the wire. For a typical Au chip wire $\tau_{fast} \sim 1\ \mu$s which is very short when compared to other timescales of the experiments and the temperature difference ΔT saturates to:

$$\Delta T(t) = \frac{hj^2\rho(\Delta T = 0)}{k - hj^2\rho}(1 - e^{-t/\tau_{fast}}). \tag{1.2}$$

The second concerns the heat transport in the substrate and is much slower: in a 2d model with a point-like heat source on the surface of a half space substrate the temperature increase is then given by

$$T_s(t) = \frac{hw\rho j^2}{2\pi\lambda}\Gamma\left(0, \frac{C_V w^2}{4\pi^2\lambda t}\right) \approx \frac{\rho I j}{2\pi\lambda}\ln\left(\frac{4\pi^2\lambda t}{C_V w^2}\right) \tag{1.3}$$

where the (small) temperature dependence of the resistivity is neglected.

These two models together accurately reproduce the results obtained in a two-dimensional numerical calculation as long as the substrate can be treated as a heat sink, which holds for short times (typically 100 ms – 1 s). For longer times the heat transport out of the substrate has to be taken into account.

Atom chip wires are typically tested using a four-point measurement, pushing a constant current through the wires while recording the change of the respective voltage drop with time. For simple single layer chips the latter is a good indicator of the change in resistivity caused by the Ohmic heating of the wires. In typical tests [5] a silicon substrate with a thin SiO_2 layer shows the lowest immediate increase of temperature, and the smallest long term heating. Silicon with a thick SiO_2 layer does show stronger heating, which is even worse for sapphire and GaAs substrates. In accordance with the above model the highest current densities are tolerated by the thinnest wires with the smallest width. A 700 nm wide and 140 nm high wires carried currents of up to 60 mA over 10 s, corresponding to a current density of $6 \times 10^7\ \mathrm{A/cm^2}$. Similar tests were recently carried out with a chip fabricated on an AlN substrate [109].

Tests of multi-layer atom chip structures (Fig. 1.21) [23] show a similar behavior, but the combination of short sub–μm wires connected to large structures, and the simultaneous current through crossing wires does lead to delicate failure modes. The resistivity change is not a firm indicator of the temperature any more because different parts of the wire contribute differently to the changes. A simple rule of how much resistivity increase one can safely tolerate cannot be applied. Limits have to be found for each individual wire category.

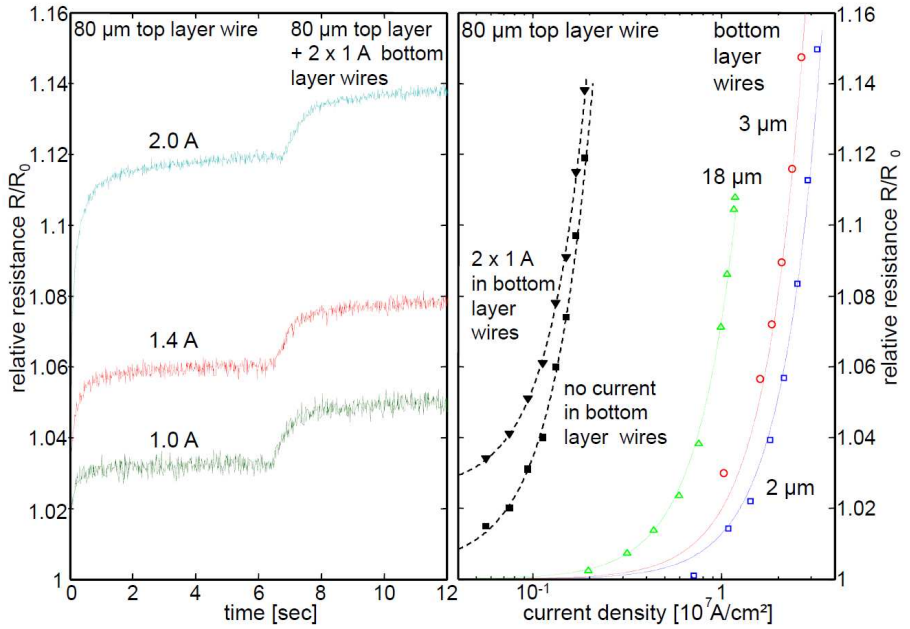

Fig. 1.21 a) Temperature evolution of a 80 μm top layer trapping wire for different applied currents. After $\sim$ 6 s, an additional current of 1 A is sent through two 500 μm bottom layer confinement wires. b) Temperature evolution for different current densities in various chip wires. Solid lines are theoretical predictions according to a simple dissipation model which applies to bottom layer wires in direct contact with the substrate [5]. Reduced heat dissipation reduces the current density for top layer wires, currents in the bottom layer wires lead to additional heating (dashed lines to guide the eye).

Finally, atom chips also create electric fields. Very small structures naturally create large electric fields. This is due to sharp corners as well as small gaps. For example, a moderate voltage of 60 V translates to an applied electric field of over 200 kV/mm over 300 nm gaps between small wires. It has been shown that atom chips can indeed sustain very high electric fields without breakdown allowing to create very steep potential surfaces and to implement versatile state selective combinations of electric and magnetic potentials [21].

1.8
Photonics on atom chips

The interaction between atoms and light is an essential ingredient in preparing, detecting and manipulating atoms. It is therefore natural to integrate micro-optics on the atom chip.

1.8.1 Fiber-based integrated optics

A simple and very well developed technology that allows to integrate light with the atom chip is fiber optics, which may be placed on the chip surface. Components that don't need active alignment, such as cavities with mirrors implanted in the fiber, or tapered fibers for dipole traps or for the delivering of excitation light, can be directly integrated on the chip, and microfabricated SU8 holding structures are the method of choice [110]. This strategy will not work well for fiber cavities which need to be actively aligned during operation; here actuators are needed.

1.8.1.1 SU8 - holding structures

SU8 [111] is an epoxy based negative photo resist which can be patterned using 365-436 nm UV-light, and which is compatible with Ultra High Vacuum requirements. It has very high mechanical, chemical, and thermal stability. Its specific properties facilitate the production of > 100 μm thick structures with very smooth sidewalls with a sizable undercut. SU8 is widely used to fabricate diverse micro-components ranging from optical planar waveguides with high thermal stability and controllable optical properties to mechanical parts such as microgears [112] for engineering applications, and microfluidic systems for chemistry [113].

To mount fibers on the chip, the Heidelberg / Vienna team fabricate two SU8 ridges which are separated by a distance a few hundreds of nanometer smaller than the fiber diameter, and have a height of typically 60% of the fiber diameter. The layout of the used alignment structure with fibers is shown in Fig. 1.22. This design includes funnels to simplify assembly. To avoid angular misalignment the total length of the alignment structure is quite long (6000 µm). The structure is divided into several subsegments to reduce stress induced by thermal expansion. The fibers can then be inserted from the top by applying a little pressure on the fiber. Inside the holding structure the fibers are held precisely by the undercut, and can be shifted longitudinally with high precision. To fix the fibers they are glued with UV cured glue.

The quality of the SU8 alignment structures can be assessed by mounting a split fiber based optical resonator, with mirrors inside the two mounted fibers. The finesse of the resonator then strongly depends on losses introduced in the gap by misalignment of the two fibers [114]. Starting with a fiber resonator with a finesse of $\mathcal{F} = 152.8 \pm 1.1$, the fiber is cut between the mirrors to introduce a gap and the new surfaces are polished. The two separate fiber pieces are then introduced into the SU8 structures and mounted with a small (< 1 μm) gap size. The finesse of the split and mounted resonator was measured to be $\mathcal{F} = 132.0 \pm 1.3$. This corresponds to a coupling loss from fiber

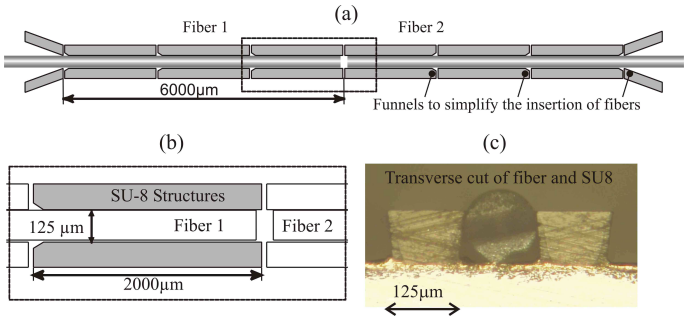

Fig. 1.22 a) Layout of the alignment structure and a magnified part (dotted rectangle) in b). c) Fiber in a SU8 structure mounted on a gold coated atom chip. The atom chip and the SU8 structures have been cut with a wafer saw. The SU8 maintains structural integrity during the cutting.

to fiber of $0.29 \pm 0.04\%$. Neglecting other additional losses, this corresponds to a transversal misalignment of < 100 nm or an angular misalignment of $< 5 \times 10^{-3}$ rad. When changing the temperature of the substrate between 20°C and 70°C the finesse of the mounted fiber resonator shows no change.

1.8.1.2 Fiber-based fluorescence detector

A simple fluorescence detector capable of high fidelity detection of single atoms can be built using a single mode tapered lensed fiber to deliver the excitation light to a very small spot and a multi-mode fiber mounted at right angle to collect the fluorescent light (Fig. 1.23). To eliminate background light and to protect the photon counter, the light passes through an interference filter before being directed to the single photon counting module (SPCM)

In the implementation by the Vienna group [116–118] the fibers are arranged at 45° to the guide and orthogonal to one another. The detector is fully integrated on the atom chip by mounting the two fibers on the chip surface in lithographically defined holders fabricated from SU8 resist guaranteeing very accurate and ultra stable passive alignment [110]. The collection fiber with NA 0.275 collects 1.9% of the fluorescence photons, and an average of 1.1 photons is counted for each atom. In the absence of atoms, less than 10^{-8} of the excitation light is scattered into the collection fiber and the a total background is dominated by the SPCM dark count rate. With such a low background a single detected photon implies that an atom is present in the detection region. With an average of 1.1 photons/atom, the detector achieved single atom detection with 66% efficiency, and a typical signal to noise ratio of 100. Most remarkable is that the stray light level is so low that atoms can propagate freely in the magnetic guide for more than a second with the detection light on, and be detected one by one when passing the detection region. The single atom de-

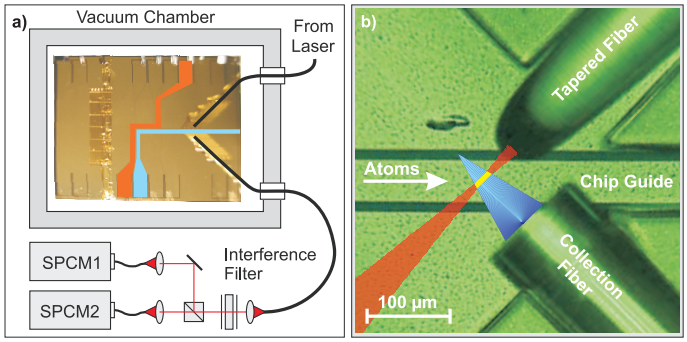

Fig. 1.23 *a)* Basic layout of the detector and the atom chip in the vacuum chamber. A magnetic guide (blue) transports the atoms from the Z-shaped wire trap (red) to the detector. The excitation light is delivered by a tapered fiber, and the fluorescence light is collected by a multimode fiber. Both are connected to the optics outside the vacuum chamber by a fiber feed-through [115]. The collected light then passes through a 3 nm wide (FWHM) interference filter centered at 780 nm before being directed to the single photon counting module(s) (SPCM). For high efficiency atom detection a single SPCM is employed while correlation measurements require two SPCMs in a Hanbury Brown-Twiss like configuration. *b)* A microscope image of the detection region on the chip. The multimode fiber collects light from a cone (blue) determined by its NA. The overlap of this cone with the excitation light from the tapered fiber (red) defines the detection region (yellow).

tection was verified by measuring the photon correlation function, and values of $g^{(2)}(0) < 0.05$ were obtained [117].

The efficiency of the detector is limited by the NA of the collection fiber, while the SNR is limited by the background. Using a low noise photon counter with a dark count rate < 25 cps, a total background of 55 cps can be achieved. Using a commercially available fiber with NA $= 0.53$ will allow to collect 4.5 photons from each atom, and a single atom detection efficiency of $\approx 95\%$ could be reached for an interaction time of 20 μs. With two detection fibers of NA $= 0.53$ and with an interaction time of 20 μs, a single atom detection efficiency beyond 99% seems feasible. Such a system would reach 9 photons/atom. This will allow true atom counting by transient count rate analysis.

1.8.1.3 Fiber cavities

The integration of high finesse optical fiber cavities on atom chips has enabled spectacular experiments on cavity quantum electrodynamics with a Bose-Einstein condensate [27] as well as high-fidelity single atom detection and preparation [119], an essential ingredient of chip-based quantum information processing (see chapter **??**). In these experiments, the atom chip allows

precise positioning of the atoms in the cavity field. Fiber cavities advantageously combine small mode volume with direct access to the high-intensity part of the intracavity field. Moreover, the light can be coupled directly in and out of the cavity through the fiber, avoiding the need for sensitive coupling optics. Here we discuss different methods to fabricate chip-based fiber cavities.

In [120–122], plano-concave microcavities are described, where the curved mirror is etched into a silicon wafer. The plane mirror is a flat, cleaved fiber tip with a high reflectivity coating applied to it, see Fig. 1.24a. Arrays of concave mirrors are fabricated in silicon by wet-etching isotropically through circular apertures in a lithographic mask using a mixture of HF and HNO_3 in acetic acid. In order to investigate cavities of various lengths, the etching parameters are adjusted to produce wafers with a range of mirror radii between 30 and 250 μm. The etched surface typically has an r.m.s. roughness of 5 nm. If the concave mirror templates are coated with sputtered gold, a cavity finesse $\mathcal{F}$ of the order of a few hundred results. Alternatively, a dielectric coating designed for 99.99% reflectivity can be used [120]. In this case, a cavity finesse of $\mathcal{F} = 6000$ can be achieved for a 15 μm long cavity, limited by the surface roughness of the curved mirror. A cavity of this kind but with $\mathcal{F} = 280$ was used for atom detection with less than one atom on average in the cavity mode [122].

A different type of fiber cavities was developed in [107, 123], see Fig. 1.24b. The cavities are of the Fabry-Pérot type and are formed with miniature spherical mirrors positioned on the end of single- or multimode optical fibers. The concave mirrors are fabricated from a convex template and a lift-off step. For large radii of curvature, $\geq$ 500 μm, the template is a commercial ball lens whereas for smaller radii, $100 - 500$ μm, a custom silica microlens with a surface roughness $\sim$ 1 nm is used. It is coated in one run with a release layer and a dielectric Bragg mirror with nominal reflectivity of 99.7%. A cleaved single mode fiber is then positioned immediately above the center of the coated lens by maximizing the back reflection of a laser beam coupled into the fiber. The fiber is then glued in place with an UV-curing epoxy, after which the application of a small force is sufficient to detach the mirror from the original substrate. The result is a fiber functionalized with a concave mirror, see Fig. 1.24b. Two fiber tips facing each other form the cavity. The finesse is $\mathcal{F} = 1000$, currently limited by the quality of the multi-layer coatings. The detection of small ensembles of cold Rb atoms guided through such a cavity on an atom chip was demonstrated in [107].

In the experiments of [27, 119], an improved fiber Fabry-Pérot cavity with a much higher finesse of $\mathcal{F} = 37000$ is used. The cavity design is based on a new laser machining process [124] where a single, focused CO_2 laser pulse creates a concave depression in the cleaved fiber surface, see Fig. 1.24c. The machining is performed in a regime where thermal evaporation occurs, while

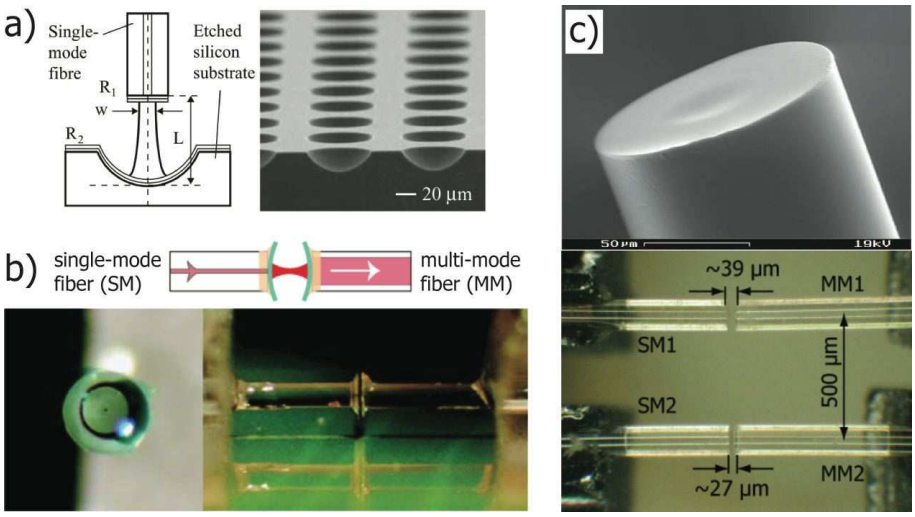

Fig. 1.24 Optical fiber cavities on atom chips. (a) Plano-concave cavity of [120, 121] with a finesse of up to $\mathcal{F} = 6000$. Left: The plane mirror is formed by coating a fiber tip, the concave mirror is formed by coating an etched silicon wafer. Right: SEM micrograph of an array of mirrors on a silicon wafer. (b) Fiber Fabry-Pérot cavity with $\mathcal{F} = 1000$ described in [107, 123]. Two fibers functionalized with a concave dielectric mirror face each other. Left photograph: a single-mode fiber processed with a concave mirror. Right: mounted cavity of 27 μm length on an atom chip. (c) Fiber Fabry-Pérot cavity with $\mathcal{F} = 37000$ used in [27, 119]. Top: SEM image of a laser-machined fiber end face. Bottom: Two fiber cavities of different length mounted on the same atom chip.

melting is restricted to a thin surface region, avoiding global contraction into a convex shape. The surface is then coated with a dielectric mirror coating.

The observed $\mathcal{F} = 37000$ is limited by the sub-optimum coating. Ultimately, a finesse of $\mathcal{F} = 150000$ should be achievable based on the measured surface roughness of about 0.2 nm r.m.s. Radii of curvature can be fabricated down to 50 μm and probably below. Because of the small mirror diameter (smaller than the fiber diameter, which is typically 125 μm), the mirrors can approach each other very closely (down to a few optical wavelengths) without touching. The result is a very small mode waist between 1 and 2 μm, and a small mode volume down to a few cubic wavelengths. These high finesse fiber cavities have enabled atom chip based cavity quantum electrodynamics experiments in the strong coupling regime as well as high fidelity single atom detection and preparation [27, 119].

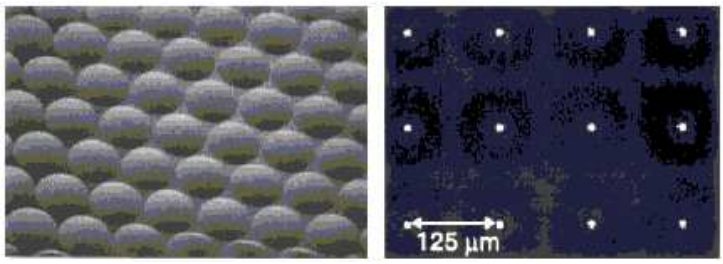

Fig. 1.25 An hexagonal array of spherical micro lenses (taken from [126]). On the right, the light intensity distribution at the focal plane.

1.8.2 Micro lens and cylindrical lens

While fibers certainly hold promise, they also posses numerous disadvantages. For example, they require alignment and gluing. Due to their radius of typically 60 microns, their interaction with atoms is usually at a similar height above the surface and this hinders the advantages of traps close to the surface (high gradients and low power consumption). To overcome this problem one would have to etch paths for the fibers within the substrate. However, the main disadvantage of fibers is in the scaling problem. Because of their size and the need for individual handling, it is hard to imagine hundreds and perhaps thousands of traps addressed individually by arrays of fibers. This has prompted an intensive effort aimed at integrating photonics into standard atom chips in order to achieve monolithic devices. The first interaction of cold atoms with substrate based optical elements was achieved in 2002 in the group of Ertmer and Birkl [125].

A review of these elements may be found in Ref. [126]. Here circular and cylindrical lenses are formed with the goal of creating dipole force traps and guides. These guides may then be combined to create beam splitters and interferometers [127]. A review of how these lenses may be fabricated can be found in Ref. [128].

1.8.3 Micro disks and toroids

The first substrate based high finesse devices to interact with cold atoms appeared in 2006 in two papers from the groups of Kimble and Vahala [129] and from the group of Mabuchi [130]. These experiments showed single atom sensitivity. To the best of our knowledge, these were also the first non fiber photonic elements of any kind to be put into the vacuum at close vicinity to the atoms. Hence, perhaps they may deserve the title of the first photonic atom chips. They were based on micro toroids sustaining a whispering gallery

mode of light [131]. These seminal experiments still used fibers (tapered) in order to couple the light into the disks and this required delicate positioning, gluing and tuning. Furthermore, no trapping of atoms has taken place in these experiments and this will presumably be aspired to in the next generation setups.

Let us review in more detail the above experiments. In the experiments performed by the Mabuchi group a quality factor of $Q \approx 10^6$ (defined as the ratio of the frequency to the line width or loss rate) was achieved by etching a 9 μm SiN disk. Here work was done with commercially available Si wafers with a 250 nm layer of SiN deposited by Low Pressure Chemical Vapor Deposition (LPCVD). A highly circular mask was made by e-beam lithography and resist reflow and was transferred to the SiN by way of C_4F_8/SF_6 plasma dry etch. Potassium hydroxide wet etch selectively removed the underlying <100> Si substrate until the SiN micro disk was supported by a small diameter Si pillar. A final cleaning step to remove organic materials from the disk surface was performed using a $H_2SO_4 : H_2O_2$ wet etch. To fine tune the disk to the atomic resonance, a series of timed etches of a 20:1 diluted 49% HF solution were employed. The resonance was shown to blue shift at a rate of 1.1 nm per minute. Further fine tuning can be achieved by temperature variations and a dependence of 0.012 nm/°C was measured.

Similar work was done in the group of Kimble [129]. Their micro toroid was developed by the group of Vahala, where quality factors exceeding $Q \approx 10^8$ were achieved by surface tension reflow following the melting of the surface with a CO_2 laser [132]. The laser, having typical intensities of 100 MW/cm^2, is centered on the disk, but because of the Si pillar, only the disk periphery is melted. Here, nanometer scale and lower surface roughness needs to be achieved. For the purposes of interacting with atoms, quality factors exceeding 10^6 were sufficient and those were realized with disk diameters of about 100 μm without the need for laser melting [133]. First, silicon wafers with 2 μm of silicon oxide thermally grown (silica) were patterned by standard optical lithograph and wet etch of the oxide using buffered HF. The silica disks were then isolated from the silicon substrate with an isotropic silicon dry etch using XeF_2 (3 Torr). Like before, the resonator is now suspended and being supported by a silicon pillar.

1.8.4 Mounted and fully integrated Fabry-Pérots

Similar to fully integrated micro disks, monolithically fabricated Fabry-Pérots (FPs) offer robustness, accuracy and scalability. As the mode volume achieved by fiber based FPs is already extremely small, it is not expected that integrated FPs would be able to decrease the mode volume by more than say factor 10

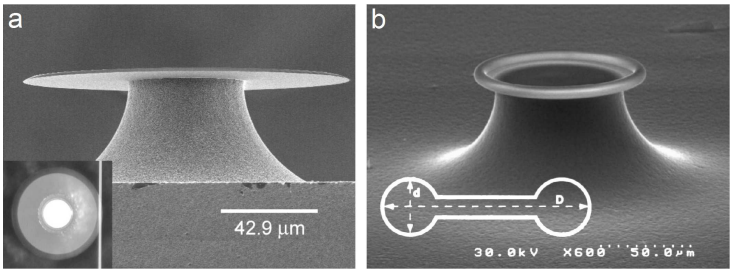

Fig. 1.26 a) A micro disk (taken from [133]). The disk itself is made of 2 μm thick oxide. The inset shows the fiber which couples the light into the micro disk. b) An ultra high finesse toroid (taken from [134]).

at most. Hence, the advantage in realizing these elements is really in the fact that they enable scalability. Different from the case of the micro disk where the atom interacts with an evanescent field, here the atom interacts with a real light mode. This may enable numerous advantages, one being the distance from a material object. Attempts to realize such optical elements are being made by several groups. This includes the Orsay group of Aspect and Westbrook where a photonic wave guide is being etched in the middle and the mirrors are realized by way of Bragg gratings implanted in the wave guide. Taking into account the interface between the waveguide and the vacuum, this forms a "double" FP of sorts and was analyzed in detail in Ref. [135]. To the best of our knowledge, the only group so far to realize a non-fiber miniature FP mounted on the surface of an atom chip is the Berkeley group of Dan Stamper-Kurn. Though not monolithically fabricated (but rather assembled), this system may already be considered as integrated. Let us briefly review their work.

The first effort [136] was made by using a sapphire substrate both as the base for the atom chip wires and also for high-reflectivity planar mirrors. The vision is to place a curved mirror above the planar "mirror pad" forming a stable mode. Here, the flat dielectric mirrors which were used were made of alternating layers of SiO_2 and Ta_2O_5 (Research Electro-Optics, Boulder) totaling about 5 μm in thickness. With a 400 nm thermally evaporated aluminium protective layer in place, Reactive Ion Etching (RIE) was used to etch away unwanted mirror areas (100 sccm CF_4 and 10-20 sccm O_2 at 85 mTorr and RF power of 0.4 W/cm^2). About 5 μm of mirror edge were lost in this process, achieving finally a finesse of about $\mathcal{F} = 10^5$.

One valuable outcome of this work is the high level of control realized over the temperature of the atom chip surface, and the discovery that one could actuate a high finesse mirror thermally to achieve a closed-loop control of the Fabry-Pérot cavity spacing with a 1 MHz bandwidth. This is a powerful new

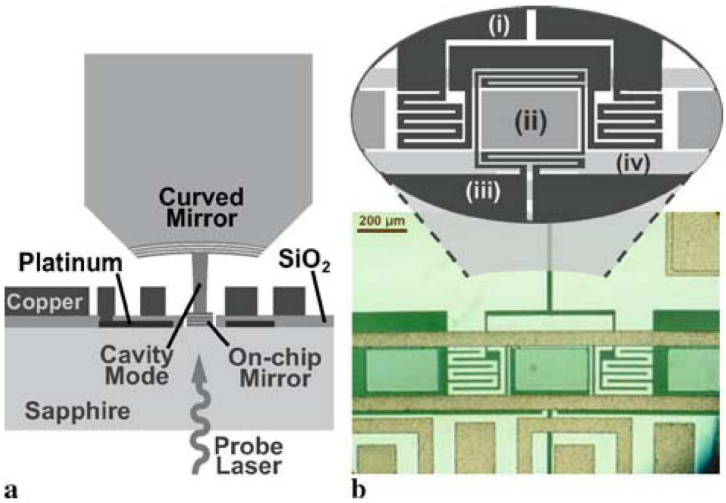

Fig. 1.27 Flat dielectric mirror on a sapphire substrate (taken from [136]). The mirror is made of a combination of alternating layers of silicon dioxide and tatalum pentoxide (see text). Around the mirror one may observe the platinum heaters for actuating the mirror. The second mirror is curved and mounted on a piezo stage. top right: (i) thermometer wire (ii) dielectric mirror pad (iii) heater wire (iv) waveguide wire.

capability which would enable robust Cavity QED since the kHz-level acoustic noise can be now suppressed immensely.

A second "cheaper" and less integrated project now under way utilizes Deep Reactive Ion Etching (DRIE) to thin down a silicon wafer to just <100 micron thickness, including the wires atop that thinned substrate. A hole is then micro-machined through this thinned wafer. Mirrors mounted on a separate piezo mounting are positioned on both sides of the chip so that a vertical cavity mode pierces through the horizontal chip surface. In this way, the mirrors are decoupled from the atom chip (useful for both thermal and vibrational isolation), and may be reused for many iterations of the atom chip. In addition one may use cheaper materials and fabrication for the chip itself.

Finally, let us note a recent result from the group of Ed Hinds at Imperial College [137] in which for the first time a fully integrated (monolithically fabricated) array of atom-light junctions has been operated (Fig. 1.28). This may be considered the first real step towards a scalable system.

1.8.5 Planar optics

Planar optics (i.e. optics with no curved surfaces) are well established, and although they are ideal for standard fabrication techniques, they have almost

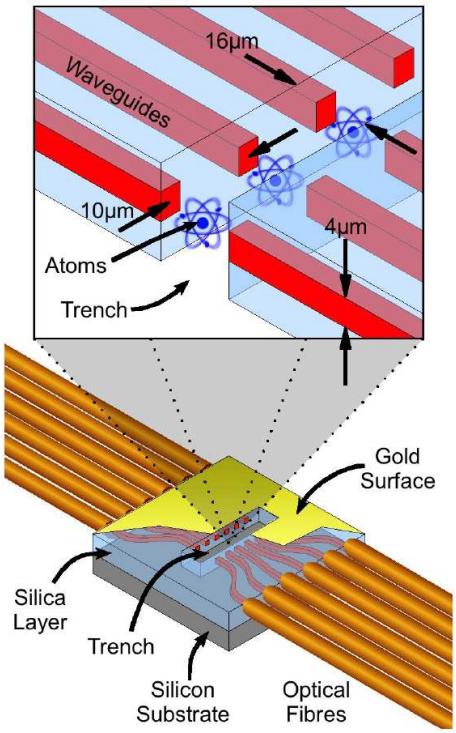

Fig. 1.28 An array of monolithically fabricated atom-light junctions [137].

not been exploited in the field of atom chips. To the best of our knowledge only one publication exists describing such work [138]. In this work by J. Weiner and H.J. Lezec, a Fresnel (diffraction) lens has been etched by a Focused Ion Beam (FIB) (Fig. 1.29). The overall size of the element is still quite large (about 200 by 200 μm^2) but the method may be considerably miniaturized. For example, it has also been suggested to trap and measure atoms via long focal length plasmon lens [139], made so far also by FIB. Here light passes the substrate through a 250 nm hole. Such holes may be produced by the beam of a FIB or electron beam induced etching (utilizing gas injectors inside an e-beam machine), as these beams have a very small diameter of several nanometers. To the best of our knowledge, while a small divergence beam has been produced by plasmon lens, a focus has not. Another idea for an extremely small planar optical element is to utilize the fast growing field of sub wavelength optics. Here, a transparent material may be etched with high aspect ratios to produce a phase mask which gives rise to optical control. As the resolution required in these elements is below that of optical lithography, and as e-beam lithography is time and price consuming, such elements will

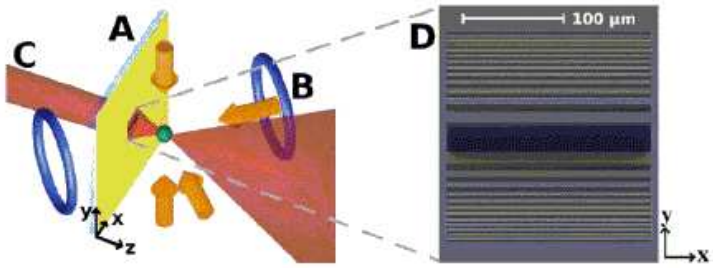

Fig. 1.29 The cold atom setup and a zoom in on the FIB etched 1d Fresnel diffraction lens (taken from [138]).

most likely be produced by nano imprint methods where a hard mask possessing the negative image is brought into contact with a soft material. The mask can, for example, be made of sapphire. Currently, DRIE protocols exist for sapphire e.g. with Nickel masks allowing for an etch selectiveness of 1:7.

1.8.6 Photonics outlook

It is clear that the eventual goal of the photonics effort should be to use light on the surface of the atom chip to trap, manipulate and measure atoms (down to a single atom) in a way that allows integration with other atom chip techniques such as magnetic traps, and utilizing configurations that require standards monolithic fabrication techniques in order to achieve robust and accurate scalability. This probably means solid state light wave guides which will transfer light from fibers glued at the edge of the chip to monolithic optical elements in the center of the chip, as in the recent achievement by the Hinds group (Fig. 1.28). Waveguides with low scattering i.e. small surface roughness, are a challenge in their own right. For example, annealing a SiO waveguide for 20 hours at 1000°C may reduce its surface roughness from several nanometer rms to less than one. The eventual goal would of course be to have no fibers at all, namely to have the light sources and the photo detectors integrated on the chip itself so that only electronics will need to interface with the chip. While the above is the general vision, it is unclear what the final "winning" monolithic optical element would be. Considering the variety of demands including also the eventual price tag, it is likely that for every specific application another type of element would perform best.

Concerning the integration of micro disks, the first issue is that of simultaneous trapping allowing for long interrogation times. Standard magnetic trapping poses the challenge of light induced spin flips to un-trapable states. In addition, a metal with a wide absorption spectrum put in the vicinity of a high finesse mode may significantly reduce its finesse. Magnetic traps based

on molecules (e.g. CNT) with very sharp absorption peaks may be one way to solve this problem. Another way may be through simultaneous optical trapping and sensing. Here blue and red modes create a potential minimum next to the disk. Counter propagating modes can create arrays of traps. A fabrication tolerance analysis of such a scenario was done in Ref. [140]. The second issue requiring development is that of tunability. So far tunability has only been done by thermal control. In Ref. [131], other tunability mechanisms have been analyzed. These include fabricating the disk from piezo material where a voltage would change the disk diameter or utilizing an Electro-Optical (EO) material where a voltage would induce a change of index. Both these options require extensive materials and fabrication development. For example, standard EO materials are crystalline in nature and may not be evaporated onto the wafer (e.g. $LiNbO_3$). Etching these materials with a high surface quality is also very challenging. A possible solution may be to use polymers with EO features that may be deposited through evaporation. A third issue is that of light coupling. While disk fabrication without the existence of a nearby wave guide enables to utilize a variety of methods to achieve high finesse (in which case a tapered fiber is later brought to the vicinity of the disk), monolithic fabrication of both disk and waveguide demand either a single step fabrication in which methods are used for the disk that do not harm the wave guide or significantly affect the gap between the two, or alternatively a double step fabrication which involves accurate alignment and reduces the yield. As parameters like the shape of the wave guide, its surface roughness and the exact dimension of the gap to the micro disk may significantly affect the light coupling and the disk finesse, the joint fabrication of these two elements is a demanding challenge.

Concerning the integration of FPs: Two issues seem to be the most challenging problems on the way to the development of such a device. The first is 3d fabrication and the second tunability. For a stable mode to exist at least one of the two mirrors must have a 3d profile or alternatively both mirrors must have a 2d profile where the overall structure is 3d. A well established fabrication protocol for 3d structures actually does not exist. There are attempts to produce 3d structures by way of controlled electron penetration and scattering within an e-beam resist. Similarly, there are attempts to utilize laser light where the focus exposes 3d structures in a photo resist. However, these are crude methods with no good control over parameters like curvatures and the surface roughness achieved so far is not good enough. Even if these problems were to be solved, there still remains the issue of how to evaporate a mirror (be it metallic or dielectric) onto these highly curved surfaces. The second issue involves tunability. Different from the case of the micro disk, here tunability would involve a real movement of the mirrors (unless some of the cavity mode is in a material, as in the above described "double" FP, in which case the

index of refraction may be changed as in the micro disks, or unless some thermal mechanism like that developed by the Dan Stamper-Kurn group may be employed). Such a movement is possible through MEMs or piezo stages, but then the interface to the waveguides bringing and taking the light becomes complex.

Aside from the above noted elements realized so far, there are also numerous other ideas in the early stage of development, and below we note three as an example. The first is photonic crystals or band gap materials. In Ref. [141], a feasibility study was done concerning atom detection via the interaction with a light mode confined in the wafer by a 2d array of holes. Here the features of the light mode are critical as there needs to be a significant component of light outside the wafer. In a second example, it has been suggested to use the evanscent field of waveguides for trapping and interacting with atoms. Two color schemes (red detuned and blue detuned) create a trapping minimum while counter propagating beams create standing waves and therefore arrays of traps. The affect of surface roughness on the feasibility of such an idea was analyzed in Ref. [140]. These ideas would require considerable fabrication development and nanometer scale control over parameters such as edge and surface roughness, as well as high aspect ratio etching. In a third example, light is confined to propagation in nano structures, and may be used for strong interaction with atoms and for efficient transport of light (see for example the work of M. Lukin, P. Hemmer, P. Zoller and others [142, 143]).

Last but not least, photonics will also include considerable work on the substrate itself. Using transparent substrates such as sapphire, one would be able to introduce planar optics such a Fresnel lens described previously or even sub-wavelength optics. 3d fabrication may also be utilized such as in the pyramid or bowl shaped substrate etching done by the Hinds group (and collaborators from Southampton) for the creation of an on-chip integrated Magneto-Optical Trap [144] or optical cavity [120, 121]. Transparent substrates may also enable evanescent blue detuned light to form stable near surface traps with charged electrodes [145].

1.9 Chip dicing, mounting and bonding

After the microstructures on an atom chip have been fabricated, the chip has to be cut to the desired size, mounted on a heat sink, integrated into a UHV vacuum chamber, and connected to the outside world. Fig. 1.30 shows examples of such complete atom chip systems.

In Fig. 1.30a, the atom chip of [20, 41] is shown. The main "experiment chip" consists in this case of two layers of gold wires on a Si substrate (cf.

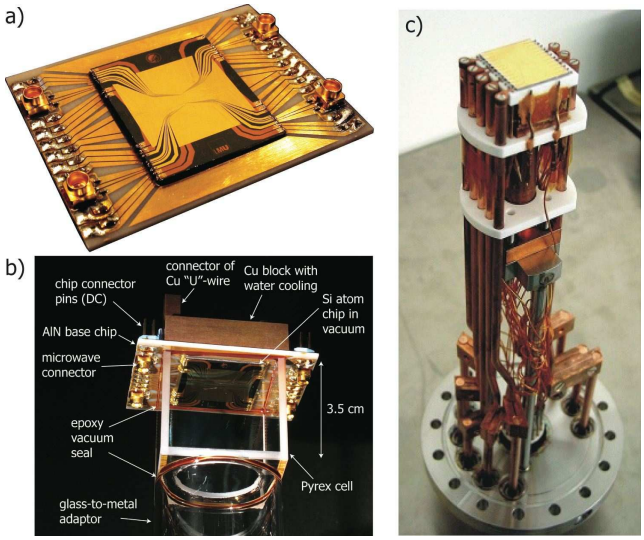

Fig. 1.30 Atom chip mounting, bonding, and contacting. (a) Multi-layer microwave atom chip of [20, 41]. The two-layer experiment chip is glued and wire bonded to a single-layer carrier chip. Microwave and DC connectors are soldered onto the front and back side of the carrier chip. (b) Atom chip shown in (a) attached to a glass cell vacuum chamber. UHV compatible epoxy seals the vacuum. (c) Atom chip system of [146]. The chip is attached to a vacuum flange with electrical feedthroughs. Copper structures behind the chip are used as a heat sink and to create large-volume traps.

Fig. 1.20). It is cut to size with a diamond blade and subsequently glued onto a "carrier chip" with larger gold wires on an AlN substrate. The carrier chip serves as a heat sink and electrical vacuum feed through. The epoxy glue is UHV-compatible, heat-conductive, but electrically insulating, and care is taken that the gap between the chips is completely filled with epoxy to avoid virtual leaks in the vacuum system. The wires on the experiment chip are wire bonded to the carrier chip, using up to 15 gold bond wires per chip wire. The carrier chip substrate has arrays of holes on each side, which were laser-cut before the wires were fabricated. The holes allow one to solder wires on the front side of the chip to pins of a connector fed through from the back side, using a 70In/30Pb reflow solder paste. A connector on the back side has the advantage that it does not inhibit optical access to the chip.

The atom chip is attached to a copper block, which is kept at a constant temperature by water cooling. Millimeter scale machined copper structures are integrated into this block. Such U- or Z-shaped metal structures are a useful tool to create large-volume quadrupole or Ioffe-Pritchard type magnetic fields in the initial trapping stages of the experiment [44, 146].

Different techniques exist to integrate atom chips into the UHV vacuum chambers required for ultracold atom experiments. One approach is to mount the atom chip assembly onto a vacuum flange with electrical feedthroughs, see Fig. 1.30c [44, 146, 147]. In the example of Fig. 1.30b, a different technique is used, in which the carrier chip is directly connected to a glass cell vacuum chamber. This technique, which was first described in [148], eliminates the need for separate electrical vacuum feedthroughs, as the carrier chip wires can be directly connected from outside the vacuum chamber. To seal the vacuum, either UHV compatible epoxy glue [41] or anodic bonding techniques [149] can be used. This technique allows one to further miniaturize ultracold atom experiments [149], and complete systems consisting of an atom chip attached to a miniaturized glass cell vacuum chamber are commercially available.

1.10 Further integration and portability

The atom chip was born in three laboratories around 1999 (Munich, Innsbruck and Boston). The vision of its makers and those who followed was of a robust and accurate, miniature and portable system that could replace the large cold atom systems. Such an achievement would not only enable subtle experiments in fundamental physics but could also enable technological applications such as clocks, sensors, and quantum information processing.

For this to happen numerous technologies must be further developed and integrated:

- Substrates: Although substrates (wafers) may seem a trivial matter, they are an extremely important issue. For example, when using standard silicon wafers, one reduces the possibility to transmit visible light through the wafer. One also adds in such a case the requirement for an insulation layer which usually conducts heat badly, thus disconnecting between the current carrying wires and their heat sink. Sapphire, for example, is transparent in the visible and does not require an insulating layer while being a good heat conductor. However, it is very hard (although possible) to etch sapphire, and adhesion to metallic layers may be more problematic. Sapphire is a good example for other considerations, as it may be used when RF with low losses is required (e.g. in ion chips). Transparent wafers also enable easy back side alignment for back side fabrication. It is very likely that any substrate used in the future will require robust deep etch processes. Vias for through-wafer electrical contacts (see following), loading wires (for magnetic loading) and loading slits (e.g. in ion chips where the particle source is likely to be on the back side of the chip), and eventually miniature vacuum cells within the wafers (closed

by anodic bonding for example) - all these would require deep and at times high aspect ratio etching.

- Metallic and insulating layers: Assuming electro-magnetic, electric, and magnetic fields will continue to play a major role in atom chips, metallic and insulation layers will continue to need improved material engineering and fabrication protocols. Numerous methods may be combined. For example, loading wires which are shut down during subtle quantum operations and which are far away from the atoms, may be made of thick layers (e.g.10-100 μm) by way of electroplating on the back side of a thin wafer (e.g. 100 μm) or in deep etched grooves on the front side of a thick wafer. Finer wires made by evaporation with thickness up to 2 μm will be put closer to atoms for traps and guides in which quantum operations take place. Here, for complex trap and guide geometries, numerous layers may evaporated with planarized insulating layers in between.

- "Exotic" materials: These pose a fabrication challenge in terms of compatibility of materials and fabrication protocols. For example, as described above, crystalline materials (e.g. electrically anisotropic materials) may prove to be very advantageous in fighting potential corrugations and spin-flip, heating and dephasing due to noise. Such materials may not be evaporated and their patterning may not be done by normal means of lift-off (of photo resist). Here techniques of shadow mask need to be employed for plasma etching or ion beam milling. Finally, integration with nanowires, molecules such as CNTs and other nano devices such as mechanical oscillators will require the integration of even more materials and fabrication techniques as described above. For example, while single wall CNTs usually grow in a Chemical Vapor Deposition (CVD) oven, delicate electrical contacts may be done by Electron Beam Induced Deposition (EBID), and contact wires by thermal evaporation which may be either done by an e-gun (in the case of paladium) or by thermal evaporation (in the case of gold).

- Photonics: The integration of photonics means that all light sources and photo detectors would eventually be on the chip so that no light connections via fibers are required. These light sources would deliver the light to the different optical systems through single or multi mode dielectric wave guides having cross sections of a few microns, or alternatively through nano structures (plasmonics), as noted in the photonics outlook section. The optical elements themselves have been discussed above and may include wave guides, micro curved lens, planar lens, and FP or micro disk cavities. Transparent substrates may also enable

evanescent blue detuned light to form stable near surface traps with charged electrodes. Atom laser cooling would also need to be miniaturized and here a single beam Magneto-Optical Trap (MOT) would perhaps be utilized. Such miniature pyramid/cone MOTs have recently been developed in several groups [144,150,151]. For effective atom cooling, manipulation and measurement, frequency lock schemes will also need to be integrated onto the chip. Indeed, recently several new miniaturized lock schemes have been suggested (e.g. see Ref. [152]).

- Electronics: To increase the signal over noise, and to reduce the amount of electrical connections to the chip, it is plausible that future chips will require some level of electronics to be integrated onto them. For example, fabrication of photo diodes and pre amplifiers for the readout, or feedback electronics and high voltage drivers for the laser lock. It stands to reason that such electronics will be fabricated on the back side of the wafer and connected to the atom optics side by means of electrical vias.

- Vacuum: The issue of miniature vacuum cells has been the focus of considerable effort and will undoubtedly continue to be so. Similar to the effort in the context of atom cells for room temperature atom optics devices made by the group of John Kitching [153], it is possible that future miniature cells will be contained inside the substrate itself. Here techniques of wafer anodic bonding, as well as deep etch and MEMs, will play a major role. Blue LEDs may also be used to achieve a fast transition from the state of bad vacuum required for good MOT loading, to the state of good vacuum required for long trap and interrogation times [154].

As an example of the state-of-the-art of miniature vacuum systems and electric contacts we present recent work from the groups of Dana Anderson and Victor Bright (Fig. 1.31) [155]. This paper describes a new method for fabricating through-wafer interconnects in atom trapping chips used in ultra-high-vacuum atom optics cells for Bose-Einstein condensation experiments. A fabrication process was developed which uses copper electroplating to seal the vias. The advantages of using feedthrough atom trapping chips are the simple microfabrication process and the reduction of the overall chip area bonded to the glass of the atom trapping cell. The results demonstrate that more than 10A of current can be conducted through the vias while the vacuum can be held at around 10^{-11} Torr pressure at room temperature. The yield rate of fabricated via interconnects in this process after anodic bonding (requires heating to 425°C) is 97%.

The group has also pioneered work on ultra low volume vacuum systems as part of an effort to complement the miniaturization of atom optics which state-of-the-art fabrication enables. In Fig. 1.32 we present their chamber.

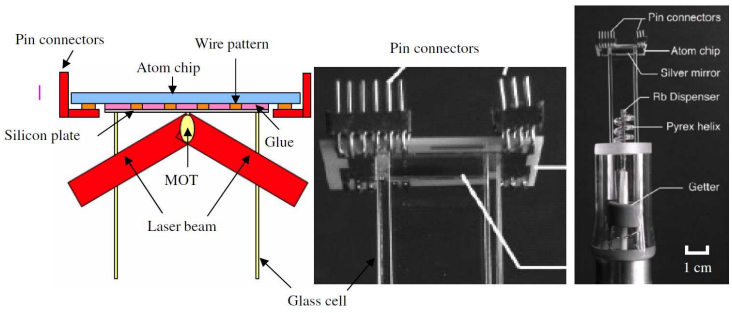

Fig. 1.31 A new atom chip configuration in which the atom chip itself is one facet of the vacuum chamber and the electrical contacts are done through the substrate by way of vias (see text for details). (taken from [155]).

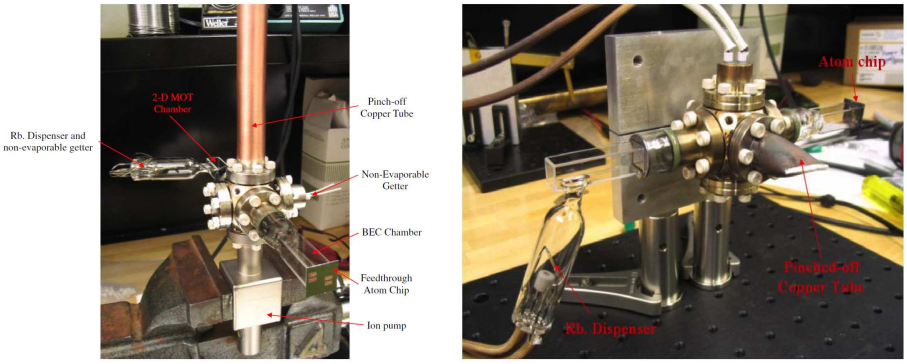

Fig. 1.32 Miniature vacuum system (taken from [155]).

We conclude this section with a beautiful illustration of a future atom chip made by Tim Freegarde of Southampton. Here one finds many of the features discussed above. Deeply etched substrate, miniature vacuum system including miniature particle sources, pumps and valves, single beam MOT, on board light sources and photo detectors, and so on.

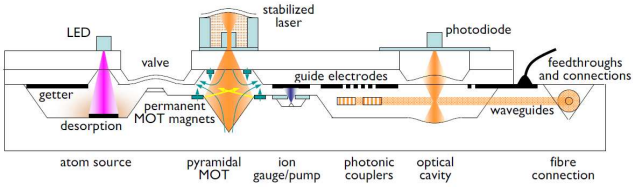

Fig. 1.33 A futuristic vision of the atom chip (courtesy of Tim Freegarde). Here all the concepts of miniature vacuum, miniature light and particle sources, photonics and micro magnetic traps, all come as an integrated device on top of one substrate.

1.11 Conclusion and outlook

Fabrication of atom chips came a long way from the simple gold layers of the first demonstration experiments. Ten years later we have numerous different technologies involved in building a chip, and new combinations are developed with each new experimental task to be implemented. This trend of utilizing the best material engineering has to offer, will continue.

The atom chip has proven to be a versatile platform in integrating different experimental technologies for quantum manipulation of atoms. Its success has led to similar developments for the manipulation of ions and molecules.

In future, an additional force driving atom chip development will be the increasing demand for integrating different quantum systems into larger hybrid quantum systems, combining the best of the quantum worlds to create a versatile quantum technology. For example integrating with the photonic quantum technology will allow atoms to be a versatile quantum memory in quantum repeater nodes for long distance quantum communications. Integrating atomic systems with superconducting quantum circuits and the emerging field of circuit QED will allow to transfer quantum information processed by MW photons into long lived hyperfine states. Integrating with nano-mechanical devices will give a way to couple and read out mechanical vibrations.

For all these one will need to constantly combine and improve the different micro and nano technologies. These continuing developments will allow the atom chip to become a genuine platform for quantum technologies.

1.12 Acknowledgments

We would like to sincerely thank Ramon Szmuk for his assistance.

Bibliography

1 R. Folman, P. Krüger, J. Schmiedmayer, J. Denschlag, and C. Henkel, *Microscopic atom optics: from wires to an atom chip*, Adv. At. Mol. Opt. Phys. **48**, 263 (2002).

2 J. Reichel, *Microchip traps and Bose-Einstein condensation*, Appl. Phys. B **74**, 469 (2002).

3 J. Fortagh and C. Zimmermann, *Magnetic microtraps for ultracold atoms*, Rev. Mod. Phys. **79**, 235 (2007).

4 M. Drndić, K. S. Johnson, J. H. Thywissen, M. Prentiss, and R. M. Westervelt, *Micro-electromagnets for atom manipulation*, Appl. Phys. Lett. **72**, 2906 (1998).

5 S. Groth, P. Krüger, S. Wildermuth, R. Folman, T. Fernholz, D. Mahalu, I. Bar-Joseph, and J. Schmiedmayer, *Atom chips: Fabrication and thermal properties*, Appl. Phys. Lett. **85**, 2980 (2004).

6 S. Wildermuth, S. Hofferberth, I. Lesanovsky, E. Haller, L. Andersson, S. Groth, I. Bar-Joseph, P. Krüger, and J. Schmiedmayer, *Microscopic magnetic-field imaging*, Nature **435**, 440 (2005).

7 S. Aigner, L. D. Pietra, Y. Japha, O. Entin-Wohlman, T. David, R. Salem, R. Folman, and J. Schmiedmayer, *Long-Range Order in Electronic Transport through Disordered Metal Films*, Science **319**, 1226 (2008).

8 T. J. Davis, *Atomic de Broglie waveguides and integrated atom optics using permanent magnets*, J. Opt. B **77**, 408 (1999).

9 M. Vengalattore, W. Rooijakkers, and M. Prentiss, *Ferromagnetic atom guide with in situ loading*, Phys. Rev. A **66**, 053403 (2002).

10 I. Barb, R. Gerritsma, Y. T. Xing, J. B. Goedkoop, and R. J. C. Spreeuw, *Creating Ioffe-Pritchard micro-traps from permanent magnetic film with in-plane magnetization*, Eur. Phys. J. D **35**, 75 (2005).

11 B. V. Hall, S. Whitlock, F. Scharnberg, P. Hannaford, and A. Sidorov, *A permanent magnetic film atom chip for Bose–Einstein condensation*, J. Phys. B **39**, 27 (2006).

12 S. Whitlock, R. Gerritsma, T. Fernholz, and R. J. C. Spreeuw, *Two-dimensional array of microtraps with atomic shift register on a chip*, New J. Phys. **11**, 023021 (2009).

13 S. W. andB. V. Hall, T. Roach, R. Anderson, M. Volk, P. Hannaford, and A. I. Sidorov, *Effect of magnetization inhomogeneity on magnetic microtraps for atoms*, Phys. Rev. A **75** (2007).

14 O. Zobay and B. M. Garraway, *Two-Dimensional Atom Trapping in Field-Induced Adiabatic Potentials*, Phys. Rev. Lett. **86**, 1195 (2001).

15 I. Lesanovsky, T. Schumm, S. Hofferberth, L. M. Andersson, P. Krüger, and J. Schmiedmayer, *Adiabatic radio frequency potentials for the coherent manipulation of matter waves*, Phys. Rev. A **73**, 033619 (2006).

16 I. Lesanovsky, S. Hofferberth, J. Schmiedmayer, and P. Schmelcher, *Manipulation of ultracold atoms in dressed adiabatic RF-potentials*, Phys. Rev. A. **74**, 033619 (2006).

17 P. Treutlein, T. W. Hänsch, J. Reichel, A. Negretti, M. A. Cirone, and T. Calarco, *Microwave potentials and optimal control for robust quantum gates on an atom chip*, Phys. Rev. A **74**, 022312 (2006).

18 P. W. Courteille, B. Deh, J. Fortagh, A. Günther, S. Kraft, C. Marzok, S. Slama, and C. Zimmermann, *Highly versatile atomic micro traps generated by multifrequency magnetic field modulation*, J. Phys. B **39**, 1055 (2006).

19 T. Schumm, S. Hofferberth, L. Andersson, S. Wildermuth, S. Groth, I. Bar-Joseph, J. Schmiedmayer, and P. Krüger, *Matter-wave interferometry in a double well on an atom chip*, Nature Phys. **1**, 57 (2005).

20 P. Böhi, M. F. Riedel, J. Hoffrogge, J. Reichel, T. W. Hänsch, and P. Treutlein, *Coherent manipulation of Bose-Einstein condensates with state-dependent microwave potentials on an atom chip*, Nature Phys. **5**, 592 (2009).

21 P. Krüger, X. Luo, M. W. Klein, K. Brugger, A. Haase, S. Wildermuth, S. Groth, I. Bar-Joseph, R. Folman, and J. Schmiedmayer, *Trapping and manipulating neutral atoms with electrostatic fields*, Phys. Rev. Lett. **91**, 233201 (2003).

22 A. Günther, M. Kemmler, S. Kraft, C. J. Vale, C. Zimmermann, and J. Fortagh, *Combined chips for atom-optics*, Phys. Rev. A **71**, 063619 (2005).

23 M. Trinker, S. Groth, S. Haslinger, S. Manz, T. Betz, I. Bar-Joseph, T. Schumm, and J. Schmiedmayer, *Multi-layer atom chips for versatile atom micro manipulation*, Appl. Phys. Lett. **92**, 254102 (2008).

24 D. Gallego, S. Hofferberth, T. Schumm, P. Krüger, and J. Schmiedmayer, *Optical lattice on an atom chip*, Opt. Lett. **34**, 3463 (2009).

25 P. Quinto-Su, M. Tscherneck, M. Holmes, and N. Bigelow, *On-chip optical detection of laser cooled atoms*, Opt. Expr. **12**, 5098 (2004).

26 X. Liu, K.-H. Brenner, M. Wilzbach, M. Schwarz, T. Fernholz, and J. Schmiedmayer, *Fabrication of alignment structures for a fiber resonator by use of deep-ultraviolet lithography*, Appl. Opt. **44**, 6857 (2005).

27 Y. Colombe, T. Steinmetz, G. Dubois, F. Linke, D. Hunger, and J. Reichel, *Strong atom-field coupling for Bose-Einstein condensates in an optical cavity on a chip*, Nature **450**, 272 (2007).

28 P. Treutlein, D. Hunger, S. Camerer, T. W. Hänsch, and J. Reichel, *Bose-Einstein Condensate Coupled to a Nanomechanical Resonator on an Atom Chip*, Phys. Rev. Lett. **99**, 140403 (2007).

29 D. Hunger, S. Camerer, T. W. Hänsch, D. König, J. P. Kotthaus, J. Reichel, and P. Treutlein, *Resonant coupling of a Bose-Einstein condensate to a micromechanical oscillator*, Phys. Rev. Lett. **104**, 143002 (2010).

30 J. Verdu, H. Zoubi, C. Koller, J. Majer, H. Ritsch, and J. Schmiedmayer, *Strong magnetic coupling of an ultracold gas to a superconducting waveguide cavity*, eprint arXiv:0809.2552 (2009).

31 J. Petrosyan, G. Bensky, G. Kurizki, I. Mazets, J. Majer, and J. Schmiedmayer, *Reversible state transfer between superconducting qubits and atomic ensembles*, Phys. Rev. A **97**, 040304 (2009).

32 A. Wallraff, D. I. Schuster, A. Blais, L. Frunzio, R. S. Huang, J. Majer, S. Kumar, S. M. Girvin, and R. J. Schoelkopf, *Strong coupling of a single photon to a superconducting qubit using circuit quantum electrodynamics*, Nature **431**, 162 (2004).

33 R. Schoelkopf and S. Girvin, *Wiring up quantum systems*, Nature **451**, 664 (2008).

34 S. Groth, *Development, fabrication, and characterisation of atom chips*, Ph.D. thesis, University of Heidelberg (2006).

35 M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*, CRC Press, New York, 2nd edn. (2002).

36 J. Reichel, W. Hänsel, and T. W. Hänsch, *Atomic Micromanipulation with Magnetic Surface Traps*, Phys. Rev. Lett. **83**, 3398 (1999).

37 W. Ruythooren, K. Attenborough, S. Beerten, P. Merken, J. Fransaer, E. Beyne, C. Van Hoof, J. De Boeck, and J. P. Celis, *Electrodeposition for the synthesis of microsystems*, J. Micromech. Microeng. **10**, 101 (2000).

38 M. Schlesinger and M. Paunovic (eds.), *Modern Electroplating*, Wiley & Sons, New York, 4th edn. (2000).

39 E. Koukharenko, Z. Moktadir, M. Kraft, M. E. Abdelsalam, D. M. Bagnall, C. Valeb, M. P. A. Jones, and E. A. Hinds, *Microfabrication of gold wires for atom guides*, Sens. Act. A **115**, 600 (2004).

40 B. Lev, *Fabrication of micro-magnetic traps for cold neutral atoms*, Quant. Inf. Comput. **3**, 450 (2003).

41 P. Treutlein, *Coherent manipulation of ultracold atoms on atom chips*, Ph.D. thesis, Ludwig-Maximilians-Universität München and Max-Planck-Institut für Quantenoptik (2008), Published as MPQ report 321.

42 J. Estève, C. Aussibal, T. Schumm, C. Figl, D. Mailly, I. Bouchoule, C. I. Westbrook, and A. Aspect, *Role of wire imperfections in micromagnetic traps for atoms*, Phys. Rev. A **70**, 043629 (2004).

43 P. Kruger, L. M. Andersson, S. Wildermuth, S. Hofferberth, E. Haller, S. Aigner, S. Groth, I. Bar-Joseph, and J. Schmiedmayer, *Potential Roughness near Lithographically Fabricated Atom Chips*, Phys. Rev. A **76**, 063621 (2007).

44 R. Folman, P. Krüger, D. Cassettari, B. Hessmo, T. Maier, and J. Schmiedmayer, *Controlling Cold Atoms using Nanofabricated Surfaces: Atom Chips*, Phys. Rev. Lett. **84**, 4749 (2000).

45 J. J. P. van Es, P. Wicke, A. H. van Amerongen, C. Rétif, S. Whitlock, and N. J. van Druten, *Box traps on an atom chip for one-dimensional quantum gases*, preprint arXiv:0911.5250 (2009).

46 K. Williams and R. Muller, *Etch rates for micromachining processing*, J. Microelectromech. Syst. **5**, 256 (1996).

47 K. R. Williams, G. Kishan, and M. Wasilik, *Etch Rates for Micromachining Processing—Part II*, J. Microelectromech. Syst. **12**, 761 (2003).

48 L. D. Pietra, S. Aigner, C. V. Hagen, S. Groth, I. Bar-Joseph, H. Lezec, and J. Schmiedmayer, *Designing potentials by sculpturing wires*, Phys. Rev. A **75**, 063604 (2007).

49 R. Salem, Y. Japha, J. Chabé, B. Hadad, M. Keil, K. Milton, and R. Folman, *Nanowire atomchip traps for sub-micron atom–surface distances*, New J. Phys. **12**, 023039 (2010).

50 J.Meingailis, J. Vac. Sci. Technol. B **5**, 469 (1987).

51 L. D. Pietra, S. Aigner, C. vom Hagen, H. J. Lezec, and J. Schmiedmayer, *Cold atoms near surfaces: designing potentials by sculpturing wires*, In *Journal of Physics: Conference Series*, vol. 19, 30–33, Institute of Physics Publishing (2005).

52 J. Fortágh, H. Ott, S. Kraft, A. Günther, and C. Zimmermann, *Surface effects in magnetic microtraps*, Phys. Rev. A **66**, 041604R (2002).

53 A. E. Leanhardt, Y. Shin, A. P. Chikkatur, D. Kielpinski, W. Ketterle, and D. E. Pritchard, *Bose-Einstein Condensates near a Microfabricated Surface*, Phys. Rev. Lett. **90**, 100404 (2003).

54 M. P. A. Jones, C. J. Vale, D. Sahagun, B. V. Hall, C. C. Eberlein, B. E. Sauer, K. Furusawa, D. Richardson, and E. A. Hinds, *Cold atoms probe the magnetic field near a wire*, J. Phys. B: At. Mol. Opt. Phys. **37**, L15 (2004).

55 J. Estève, C. Aussibal, T. Schumm, C. Figl, D. Mailly, I. Bouchoule, C. I. Westbrook, and A. Aspect1, *Role of wire imperfections in micromagnetic traps for atoms*, Phys. Rev. A **70**, 043629 (2004).

56 T. Schumm, J. Estève, C. Figl, J.-B. Trebbia, C. Aussibal, H. Nguyen, D. Mailly, I. Bouchoule, C. I. Westbrook, and A. Aspect, *Atom chips in the real world: the effects of wire corrugation*, Eur. Phys. J. D **32**, 171 (2005).

57 S. Kraft, A. Günther, H. Ott, D. Wharam, C. Z. J., and Fortágh, *Anomalous longitudinal magnetic field near the surface of copper conductors*, J. Phys. B **35**, L469 (2002).

58 D.-W. Wang, M. D. Lukin, and E. Demler, *Disordered Bose-Einstein Condensates in Quasi-One-Dimensional Magnetic Microtraps*, Phys. Rev. Lett. **92** (2004).

59 P. Krüger, L. M. Andersson, S. Wildermuth, S. Hofferberth, E. Haller, S. Aigner, S. Groth, I. Bar-Joseph, and J. Schmiedmayer, *Disorder Potentials near Lithographically Fabricated Atom Chips*, eprint arXiv:cond-mat/0504686 (2004).

60 S. Wildermuth, S. Hofferberth, I. Lesanovsky, S. Groth, I. Bar-Joseph, P. Krüger, and J. Schmiedmayer, *Sensing electric and magnetic fields with Bose-Einstein Condensates*, Appl. Phys. Lett. **88**, 264103 (2006).

61 M. P. A. Jones, C. J. Vale, D. Sahagun, B. V. Hall, and E. A. Hinds, *Spin coupling between cold atoms and the thermal fluctuations of a metal surface*, Phys. Rev. Lett. **91**, 080401 (2003).

62 P. Krüger, *Coherent matter waves near surfaces*, Ph.D. thesis, University of Heidelberg (2004).

63 Y. Japha, O. Entin-Wohlman, T. David, R. Salem, S. Aigner, J. Schmiedmayer, and R. Folman, *Model for organized current patterns in disordered conductors*, Phys. Rev. B **77** (2008).

64 R. Folman, P. Krueger, J. Schmiedmayer, J. Denschlag, and C. Henkel, *Advances in Atomic*, Mol. Opt. Phys. **48**, 263 (2002).

65 T. Varpula and T. Poutanen, *Magnetic field fluctuations arising from thermal motion of electric charge in conductors*, J. Appl. Phys. **55**, 4015 (1984).

66 C. Henkel, S. Pötting, and M. Wilkens, *Loss and heating of particles in small and noisy traps*, Appl. Phys. B **69**, 379 (1999).

67 J. Sidles, J. Garbini, W. Dougherty, and S. H. Chao, *The classical and quantum theory of thermal magnetic noise, with applications in spintronics and quantum microscopy*, Proc. IEEE **91**, 799 (2003).

68 S. Scheel, P. Rekdal, P. Knight, and E. Hinds, *Atomic spin decoherence near conducting and superconducting films*, Phys. Rev. A **72**, 42901 (2005).

69 D. Harber, J. McGuirk, J. Obrecht, and E. Cornell, *Thermally induced losses in ultra-cold atoms magnetically trapped near room-temperature surfaces*, J. Low Temp. Phys. **133**, 229 (2003).

70 Y. Lin, I. Teper, C. Chin, and V. Vuletić, *Impact of the Casimir-Polder Potential and*

Johnson Noise on Bose-Einstein Condensate Stability Near Surfaces, Phys. Rev. Lett. **92**, 050404 (2004).

71 V. Dikovsky, Y. Japha, C. Henkel, and R. Folman, *Reduction of magnetic noise in atom chips by material optimization*, Eur. Phys. J. D **35**, 87 (2005).

72 Y.-J. Lin, private communications.

73 B. Skagerstam, U. Hohenester, A. Eiguren, and P. Rekdal, *Spin decoherence in superconducting atom chips*, Phys. Rev. Lett. **97**, 70401 (2006).

74 P. Rekdal and B. Skagerstam, *Decay processes in the presence of thin superconducting films*, Phys. Rev. A **75**, 22904 (2007).

75 B. Skagerstam and P. Redkal, *Photon emission near superconducting bodies*, Phys. Rev. A **76**, 052901 (2007).

76 U. Hohenester, A. Eiguren, S. Scheel, and E. Hinds, *Spin-flip lifetimes in superconducting atom chips: Bardeen-Cooper-Schrieffer versus Eliashberg theory*, Phys. Rev. A **76**, 33618 (2007).

77 T. Nirrengarten, A. Qarry, C. Roux, A. Emmert, G. Nogues, M. Brune, J.-M. Raimond, and S. Haroche, *Realization of a Superconducting Atom Chip*, Phys. Rev. Lett. **97**, 200405 (2006).

78 C. Roux, A. Emmert, A. Lupascu, T. Nirrengarten, G. Nogues, M. Brune, J. M. Raimond, and S. Haroche, *BEC on a superconducting atom chip*, Eur. Phys. Lett. **81**, 56004 (2008).

79 T. Mukai, C. Hufnagel, A. Kasper, T. Meno, A. Tsukada, K. Semba, and F. Shimizu, *Persistent supercurrent atom chip*, Phys. Rev. Lett. **98**, 260407 (2007).

80 B. Zhang, C. Henkel, E. Haller, S. Wildermuth, S. Hofferberth, P. Krüger, and J. Schmiedmayer, *Relevance of sub-surface chip layers for the lifetime of magnetically trapped atoms*, Eur. Phys. J. D **35**, 97 (2005).

81 F. Shimizu, C. Hufnagel, and T. Mukai, *Stable Neutral Atom Trap with a Thin Superconducting Disc*, Phys. Rev. Lett. **103**, 253002 (2009).

82 T. Müller, X. Wu, A. Mohan, A. Eyvazov, Y. Wu, and R. Dumke, *Towards a guided atom interferometer based on a superconducting atom chip*, New J. Phys. **10**, 073006 (2008).

83 T. Müller, B. Zhang, R. Fermani, K. Chan, Z. Wang, C. Zhang, M. Lim, and R. Dumke, *Trapping of ultra-cold atoms with the magnetic field of vortices in a thin film superconducting micro-structure*, Arxiv preprint arXiv:0910.2332 (2009).

84 T. M
"uller, B. Zhang, R. Fermani, K. Chan, Z. Wang, C. Zhang, M. Lim, and R. Dumke, *Trapping of ultra-cold atoms with the magnetic field of vortices in a thin film superconducting micro-structure*, Arxiv preprint arXiv:0910.2332 (2009).

85 D. Cano, B. Kasch, H. Hattermann, R. Kleiner, C. Zimmermann, D. Koelle, and J. Fortágh, *Meissner effect in superconducting microtraps*, Phys. Rev. Lett. **101**, 183006 (2008).

86 D. Cano, B. Kasch, H. Hattermann, D. Koelle, R. Kleiner, C. Zimmermann, and J. Fortágh, *Impact of the Meissner effect on magnetic microtraps for neutral atoms near superconducting thin films*, Phys. Rev. A **77**, 63408 (2008).

87 V. Dikovsky, V. Sokolovsky, B. Zhang, C. Henkel, and R. Folman, *Superconducting atom chips: advantages and challenges*, Eur. Phys. J. D **51**, 247 (2009).

88 B. Lev, Y. Lassailly, C. Lee, A. Scherer, and H. Mabuchi, *Atom mirror etched from a hard drive*, Appl. Phys. Lett. **83** (2003).

89 C. D. J. Sinclair, J. A. Retter, E. A. Curtis, B. V. Hall, I. L. Garcia, S. Eriksson, B. E. Sauer, and E. A. Hinds, *Cold atoms in videotape micro-traps*, Eur. Phys. J. D **35**, 105 (2005).

90 S. Eriksson, F. Ramirez-Martinez, E. A. Curtis, B. E. Sauer, P. W. Nutter, E. W. Hill, and E. A. Hinds, *Micron-sized atom traps made from magneto-optical thin films*, Appl. Phys. B **79**, 811 (2004).

91 Y. T. Xing, A. Eljaouhari, I. Barb, R. Gerritsma, R. J. C. Spreeuw, and J. B. Goedkoop, *Hard magnetic FePt films for atom chips*, Phys. stat. sol. (c) **1**, 3702 (2004).

92 R. Gerritsma, S. Whitlock, T. Fernholz, H. Schlatter, J. A. Luigjes, J. U. Thiele, J. B. Goedkoop, and R. J. C. Spreeuw, *Lattice of microtraps for ultracold atoms based on patterned magnetic films*, Phys. Rev. A **76**, 33408 (2007).

93 Y. T. Xing, I. Barb, R. Gerritsma, R. J. C. Spreeuw, H. Luigjes, Q. F. Xiao, C. Retif,

and J. B. Goedkoop, *Fabrication of magnetic atom chips based on FePt*, J. Magn. Magn. Mater. **313**, 192 (2007).

94 J. Y. Wang, S. Whitlock, F. Scharnberg, D. S. Gough, A. I. Sidorov, R. J. McLean, and P. Hannaford, *Perpendicularly magnetized, grooved GdTbFeCo microstructures*, J. Phys. D **38**, 4015 (2005).

95 M. Singh, M. Volk, A. Akulshin, A. Sidorov, R. McLean, and P. Hannaford, *One-dimensional lattice of permanent magnetic microtraps for ultracold atoms on an atom chip*, J. Phys. B **41**, 065301 (2008).

96 V. Peano, M. Thorwart, A. Kasper, and R. Egger, *Nanoscale atomic waveguides with suspended carbon nanotubes*, Appl. Phys. B **81**, 1075 (2005).

97 R. Fermani, S. Scheel, and P. Knight, *Trapping cold atoms near carbon nanotubes: Thermal spin flips and Casimir-Polder potential*, Phys. Rev. A **75**, 62905 (2007).

98 P. Petrov, S. Machluf, S. Younis, R. Macaluso, T. David, B. Hadad, Y. Japha, M. Keil, E. Joselevich, and R. Folman, *Trapping cold atoms using surface-grown carbon nanotubes*, Phys. Rev. A **79**, 43403 (2009).

99 A. Ismach, L. Segev, E. Wachtel, and E. Joselevich, *Atomic-step-templated formation of single wall carbon nanotube patterns*, Angewandte Chemie International Edition **43**, 6140 (2004).

100 A. Ismach, D. Kantorovich, and E. Joselevich, *Carbon nanotube graphoepitaxy: Highly oriented growth by faceted nanosteps*, J. Am. Chem. Soc. **127**, 11554 (2005).

101 X. M. H. Huang, R. Caldwell, L. Huang, S. C. Jun, M. Huang, M. Y. Sfeir, S. P. O'Brien, and J. Hone, *Controlled placement of individual carbon nanotubes*, Nano Lett. **5**, 1515 (2005).

102 B. Grüner, M. Jag, A. Stibor, G. Visanescu, M. Häffner, D. Kern, A. Günther, and J. Fortágh, *Integrated atom detector based on field ionization near carbon nanotubes*, gas] (2009).

103 T. David, Y. Japha, V. Dikovsky, R. Salem, C. Henkel, and R. Folman, *Magnetic interactions of cold atoms with anisotropic conductors*, Eur. Phys. J. D **48**, 321 (2008).

104 S. R. Wilson and C. J. Tracy (eds.), *Handbook of Multilevel Metallization for Integrated Circuits: Materials, Technology, and Applications*, Noyes Publications, Westwood, New Jersey, U.S.A. (1993).

105 S. Schneider, A. Kasper, C. V. Hagen, M. Bartenstein, B. Engeser, T. Schumm, I. Bar-Joseph, R. Folman, L. Feenstra, and J. Schmiedmayer, *Bose-Einstein Condensation in a Simple Microtrap*, Phys. Rev. A **67**, 023612 (2003).

106 J. Reichel, W. Hänsel, P. Hommelhoff, and T. W. Hänsch, *Applications of integrated magnetic microtraps*, Appl. Phys. B **72**, 81 (2001).

107 T. Steinmetz, A. Balocchi, Y. Colombe, D. Hunger, T. W. Hänsch, R. J. Warburton, and J. Reichel, *Stable fiber-based Fabry-Pérot cavity*, Appl. Phys. Lett. **89**, 111110 (2006).

108 R. Long, T. Rom, W. Hänsel, T. W. Hänsch, and J. Reichel, *Long distance magnetic conveyor for precise positioning of ultracold atoms*, Eur. Phys. J. D **35**, 125 (2005).

109 J. Armijo, A. C. Garridor, and I. Bouchoule, *Thermal properties of AlN-based atom chips*, Eur. Phys. J. D **56**, 33 (2010).

110 X. Liu, K.-H. Brenner, M. Wilzbach, M. Schwarz, T. Fernholz, and J. Schmiedmayer, *Fabrication of alignment structures for a fiber resonator by use of deep-ultraviolet lithography*, Appl. Opt. **44**, 6857 (2005).

111 A. del Campo and C. Greiner, *SU-8: a photoresist for high-aspect-ratio and 3D submicron lithography*, J. Micromech. Microeng. **17**, R81 (2007).

112 V. Seidemann, J. Rabe, M. Feldmann, and S. Büttgenbach, *SU8-micromechanical structures with in situ fabricated movable parts*, Microsyst. Tech. **8**, 348 (2002).

113 D. Duffy, J. M. O. Schueller, and G. Whitesides, *Rapid Prototyping of Microfluidic Systems in Poly(dimethylsiloxane)*, Anal. Chem. **70**, 4974 (1998).

114 M. Wilzbach, A. Haase, M. Schwarz, D. Heine, K. Wicker, X. Liu, K.-H. Brenner, S. Groth, T. Fernholz, B. Hessmo, and J. Schmiedmayer, *Detecting Neutral Atoms on an Atom Chip*, Fortschr. Phys. **54**, 746 (2006).

115 E. R. I. Abraham and E. A. Cornell, *Teflon Feedthrough for Coupling Optical Fibers Into Ultrahigh Vacuum Systems*, Appl. Opt. **37**, 1762 (1998).

116 M.Wilzbach, D. Heine, S. Groth, X. Liu, B. Hessmo, and J. Schmiedmayer, *A simple*

integrated single-atom detector, Opt. Lett. **34**, 259 (2009).

117 D. Heine, M.Wilzbach, B. Hessmo, and J. Schmiedmayer, *Single-atom detector: photon and atom statistics*, Phys. Rev. A **97**, 021804 R (2009).

118 D. Heine, W. Rohringer, D. Fischer, M. Wilzbach, T. Raub, S. Loziczky, X. Liu, S. Groth, B. Hessmo, and J. Schmiedmayer, *A single atom detector integrated on an atom chip: fabrication, characterization and application*, eprint arXiv:1002.1573 (2010).

119 R. Gehr, J. Volz, G. Dubois, T. Steinmetz, Y. Colombe, B. L. Lev, R. Long, J. Estève, and J. Reichel, *Cavity-based single atom preparation and high-fidelity hyperfine state readout*, to be published in Phys. Rev. Lett., preprint arXiv:1002.4424 (2010).

120 M. Trupke, E. A. Hinds, S. Eriksson, E. A. Curtis, Z. Moktadir, E. Kukharenka, and M. Kraft, *Microfabricated high-finesse optical cavity with open access and small volume*, Appl. Phys. Lett. **87**, 211106 (2005).

121 S. Eriksson, M. Trupke, H. F. Powell, D. Sahagun, C. D. J. Sinclair, E. A. Curtis, B. E. Sauer, E. A. Hinds, Z. Moktadir, and C. O. Gollasch, *Integrated optical components on atom chips*, Eur. Phys. J. D **35**, 135 (2005).

122 M. Trupke, J. Goldwin, B. Darquié, G. Dutier, S. Eriksson, J. P. Ashmore, and E. A. Hinds, *Atom detection and photon production in a scalable, open, optical microcavity*, Phys. Rev. Lett. **99**, 63601 (2007).

123 T. Steinmetz, *Resonator-Quantenelektrodynamik auf einem Mikrofallenchip*, Ph.D. thesis, Ludwig-Maximilians-Universität München and Max-Planck-Institut für Quantenoptik (2008).

124 D. Hunger, T. Steinmetz, Y. Colombe, C. Deutsch, T. W. Hänsch, and J. Reichel, *Fiber Fabry-Perot cavity with high finesse*, accepted for publication in New J. Phys. (2010).

125 R. Dumke, M. Volk, T. Müther, F. Buchkremer, G. Birkl, and W. Ertmer, *Micro-optical realization of arrays of selectively addressable dipole traps: a scalable configuration for quantum computation with atomic qubits*, Phys. Rev. Lett. **89**, 97903 (2002).

126 G. Birkl, F. Buchkremer, R. Dumke, and W. Ertmer, *Atom optics with microfabricated optical elements*, Opt. Commun. **191**, 67 (2001).

127 R. Dumke, T. Müther, M. Volk, W. Ertmer, and G. Birkl, *Interferometer-type structures for guided atoms*, Phys. Rev. Lett. **89**, 220402 (2002).

128 N. F. Borrelli, *Microoptics Technology: fabrication and applications of lens arrays and devices*, CRC (1999).

129 T. Aoki, B. Dayan, E. Wilcut, W. Bowen, A. Parkins, T. Kippenberg, K. Vahala, and H. Kimble, *Observation of strong coupling between one atom and a monolithic microresonator*, Nature **443**, 671 (2006).

130 P. E. Barclay, K. Srinivasan, O. Painter, B. Lev, and H. Mabuchi, *Integration of fiber-coupled high-Q SiNx microdisks with atom chips*, Appl. Phys. Lett. **89** (2006).

131 M. R. andP. Horak, S. Helsby, and R. Folman, *Single-atom detection using whispering-gallery modes of microdisk resonators*, Phys. Rev. A **70**, 53808 (2004).

132 D. Armani, T. Kippenberg, S. Spillane, and K. Vahala, *Ultra-high-Q toroid microcavity on a chip*, Nature **421**, 925 (2003).

133 T. Kippenberg, S. Spillane, D. Armani, and K. Vahala, *Fabrication and coupling to planar high-Q silica disk microcavities*, Appl. Phys. Lett. **83**, 797 (2003).

134 S. Spillane, T. Kippenberg, K. Vahala, K. Goh, E. Wilcut, and H. Kimble, *Ultrahigh-Q toroidal microresonators for cavity quantum electrodynamics*, Phys. Rev. A **71**, 13817 (2005).

135 P. Horak, B. G. Klappauf, A. Haase, R. Folman, J. Schmiedmayer, P. Domokos, and E. Hinds, *Possibility of single-atom detection on a chip*, Phys. Rev. A **67**, 43806 (2003).

136 T. Purdy and D. Stamper-Kurn, *Integrating cavity quantum electrodynamics and ultracold-atom chips with on-chip dielectric mirrors and temperature stabilization*, Appl. Phys. B **90**, 401 (2008).

137 M. Kohnen, M. Succo, P. Petrov, R. Nyman, M. Trupke, and E. Hinds, *An integrated atom-photon junction*, Arxiv preprint arXiv:0912.4460 (2009).

138 G. Gay, O. Alloschery, B. V. de Lesegno, C. OŠDwyer, J. Weiner, and H. Lezec, *Optical Response of Nanostructured Surfaces:*

Experimental Investigation of the Composite Diffracted Evanescent Wave Model (2006).

139 H. Lezec, A. Degiron, E. Devaux, R. Linke, L. Martin-Moreno, F. Garcia-Vidal, and T. Ebbesen, *Beaming light from a subwavelength aperture*, Science **297**, 820 (2002).

140 M. Rosenblit, Y. Japha, P. Horak, and R. Folman, *Simultaneous optical trapping and detection of atoms by microdisk resonators*, Phys. Rev. A **73**, 63805 (2006).

141 B. Lev, K. Srinivasan, P. Barclay, O. Painter, and H. Mabuchi, *Feasibility of detecting single atoms using photonic bandgap cavities*, Nanotechnology **15**, S556 (2004).

142 A. Akimov, A. Mukherjee, C. Yu, D. Chang, A. Zibrov, P. Hemmer, H. Park, and M. Lukin, *Generation of single optical plasmons in metallic nanowires coupled to quantum dots*, Nature **450**, 402 (2007).

143 D. Chang, J. Thompson, H. Park, V. Vuletić, A. Zibrov, P. Zoller, and M. Lukin, *Trapping and manipulation of isolated atoms using nanoscale plasmonic structures*, Phys. Rev. Lett. **103**, 123004 (2009).

144 M. Trupke, F. Ramirez-Martinez, E. Curtis, J. Ashmore, S. Eriksson, E. Hinds, Z. Moktadir, C. Gollasch, M. Kraft, G. V. Prakash, et al., *Pyramidal micromirrors for microsystems and atom chips*, Appl. Phys. Lett. **88**, 071116 (2006).

145 A. Shevchenko, T. Lindvall, I. Tittonen, and M. Kaivola, *Microscopic electro-optical atom trap on an evanescent-wave mirror*, Eur. Phys. J. D **28**, 273 (2004).

146 S. Wildermuth, P. Krüger, C. Becker, M. Brajdic, S. Haupt, A. Kasper, R. Folman, and J. Schmiedmayer, *Optimized magneto-optical trap for experiments with ultracold atoms near surfaces*, Phys. Rev. A **69**, 030901 (2004).

147 W. Hänsel, P. Hommelhoff, T. W. Hänsch, and J. Reichel, *Bose-Einstein condensation on a microelectronic chip*, Nature **413**, 498 (2001).

148 S. Du, M. B. Squires, Y. Imai, L. Czaia, R. Saravanan, V. Brigh, J. Reichel, T. W. Hänsch, and D. Z. Anderson, *Atom-Chip Bose-Einstein condensation in a portable vacuum cell*, Phys. Rev. A **70**, 053606 (2004).

149 D. M. Farkas, K. M. Hudek, E. A. Salim, S. R. Segal, M. B. Squires, and D. Z. Anderson, *A Compact, Transportable, Microchip-Based System for High Repetition Rate Production of Bose-Einstein Condensates*, preprint arXiv:0912.0553 (2009).

150 K. Lee, J. Kim, H. Noh, and W. Jhe, *Single-beam atom trap in a pyramidal and conical hollow mirror*, Opt. Lett. **21**, 1177 (1996).

151 J. Kim, K. Lee, H. Noh, W. Jhe, and M. Ohtsu, *Atom trap in an axicon mirror*, Opt. Lett. **22**, 117 (1997).

152 D. Groswasser, A. Waxman, M. Givon, G. Aviv, Y. Japha, M. Keil, and R. Folman, *Retroreflecting polarization spectroscopy enabling miniaturization*, Rev. Sci. Inst. **80**, 093103 (2009).

153 L. A. Liew, S. Knappe, J. Moreland, H. Robinson, L. Hollberg, and J. Kitching, *Microfabricated alkali atom vapor cells*, Appl. Phys. Lett. **84**, 2694 (2004).

154 S. Aubin, M. Extavour, S. Myrskog, L. LeBlanc, J. Esteve, S. Singh, P. Scrutton, D. McKay, R. McKenzie, I. Leroux, et al., *Trapping fermionic 40 K and bosonic 87 Rb on a chip*, J. Low Temp. Phys. **140**, 377 (2005).

155 H. C. R. Chuang, D. Z. Anderson, and V. M. Bright, *The fabrication of through-wafer interconnects in silicon substrates*, J. Micromech. Microeng. **18**, 045003 (2008).